



Ultra Low-Power Electronics Technology

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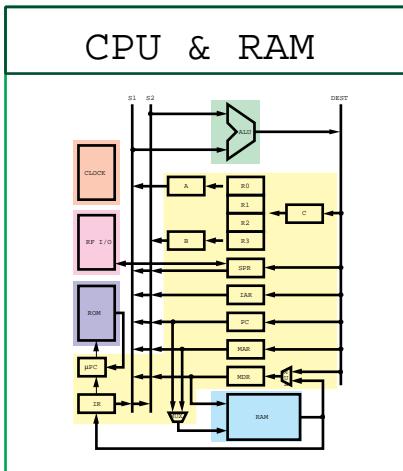
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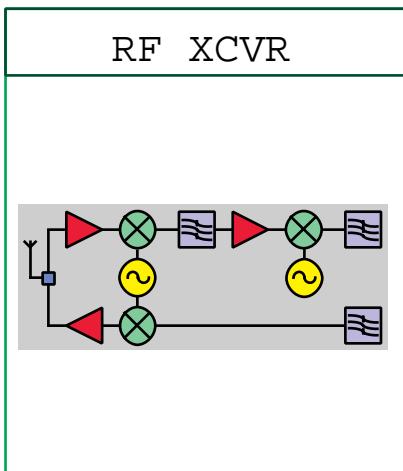


Functional Integration Applications



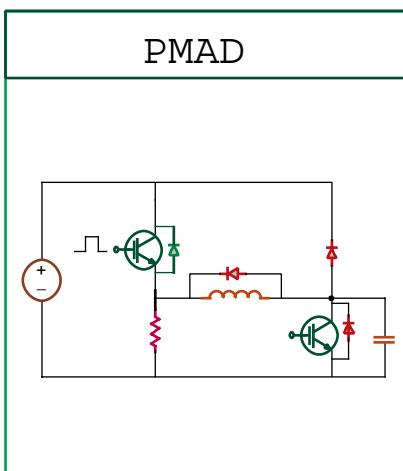
Computing

- high-performance desktop systems
- ultra-low power systems for portable use
- multimedia applications
- scientific and numerical computing



Communications

- monolithic transceiver architectures
- transceiver integration with digital processing or computing cores
- cellular phones, pages, and modems
- wireless computing



Power

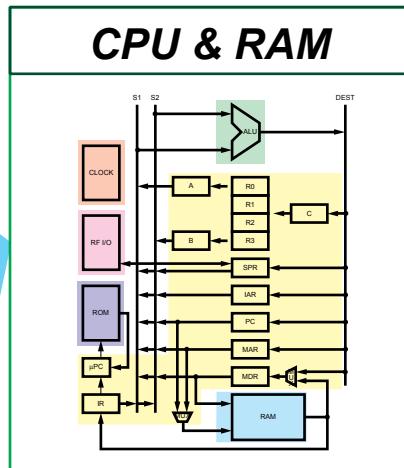
- integrated control electronics
- on-chip power conversion and regulation
- efficient portable electronics

Industries

- Intel
- IBM
- LSI Logic
- Micron
- TI
- Hitachi
- Toshiba
- Motorola
- AT&T
- US Robotics
- Tellabs
- Lucent
- National Semiconductor
- JPL/NASA



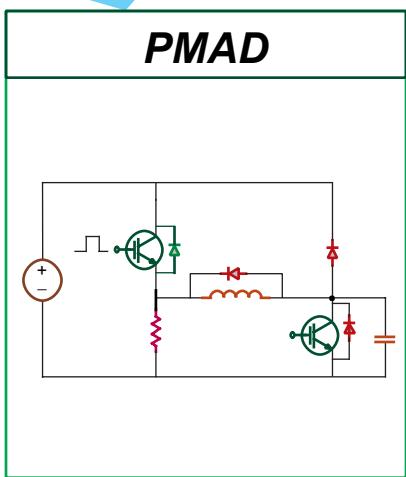
Systems on a Chip Research Activity



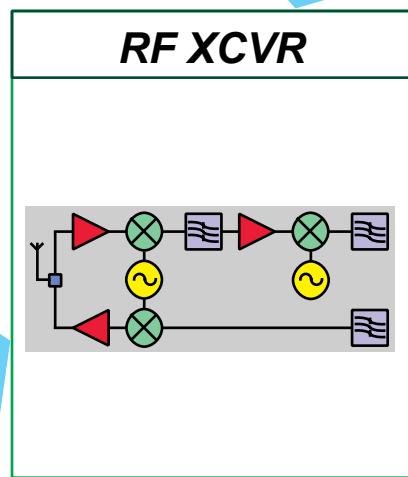
ultra-low power management
digital control of power systems



RF CMOS technology
digital transceiver circuits

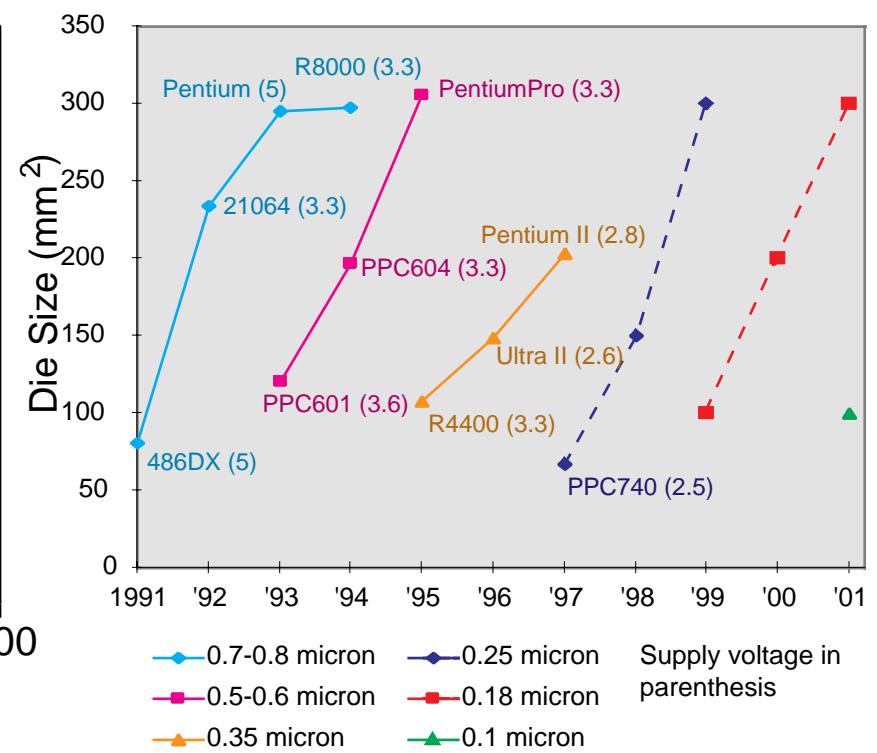
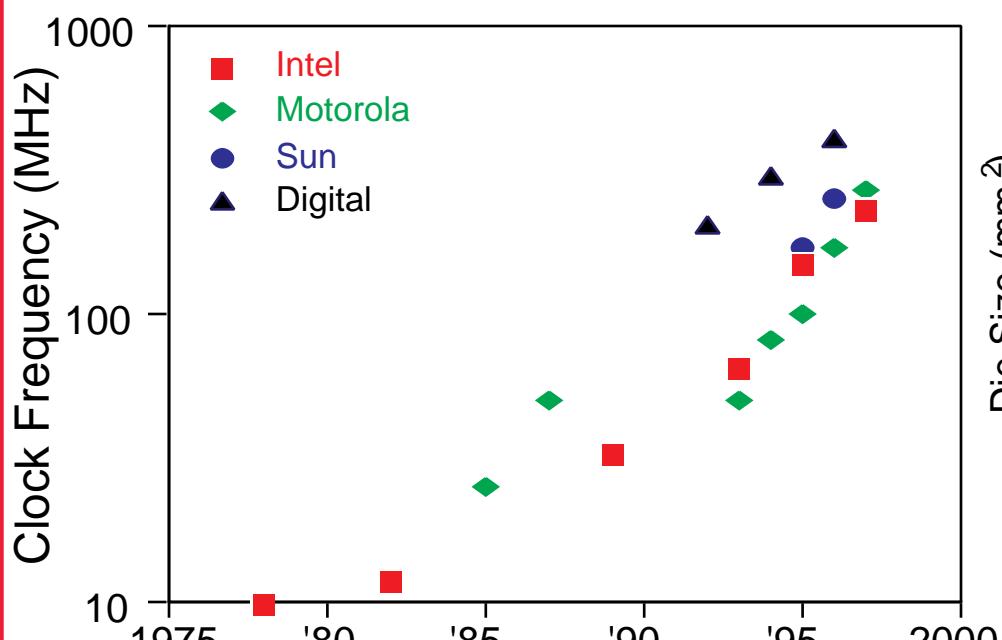


integrated magnetics
dynamic sleep mode

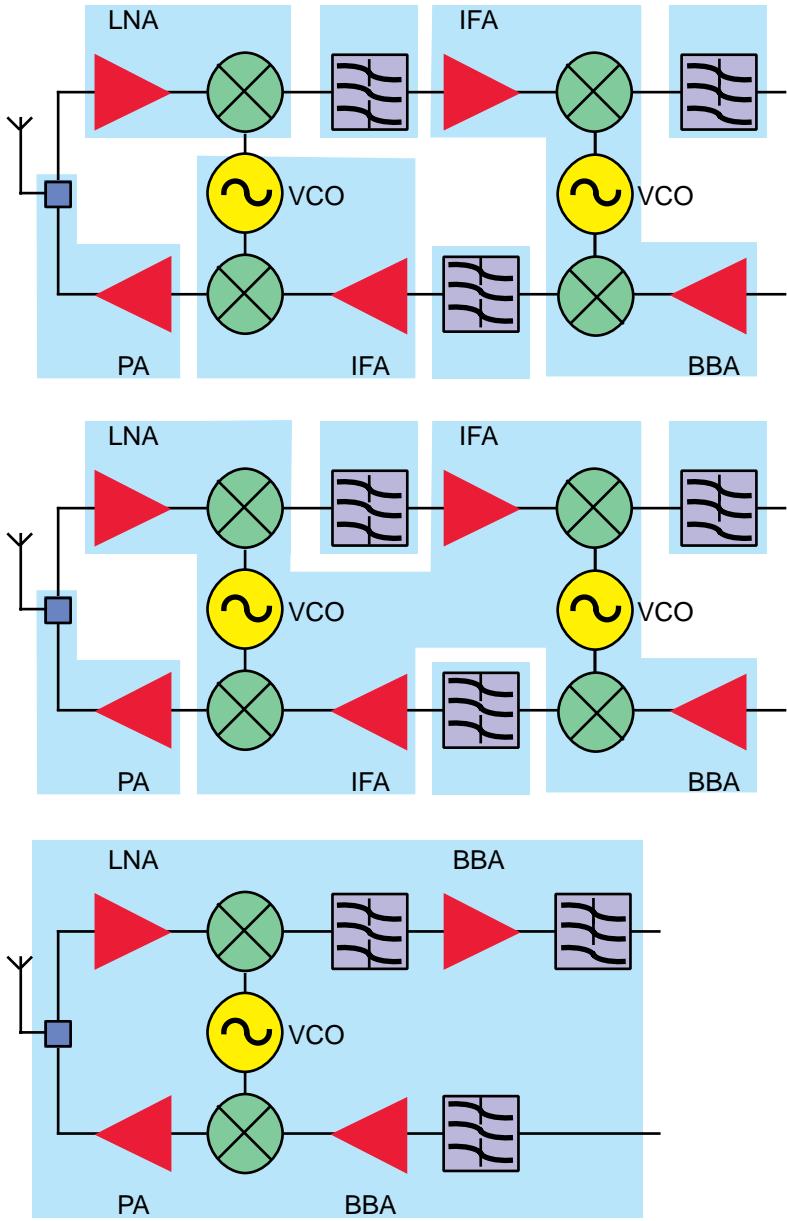




Frequency and Lithography Scaling in Microprocessors



RF Transceiver Integration



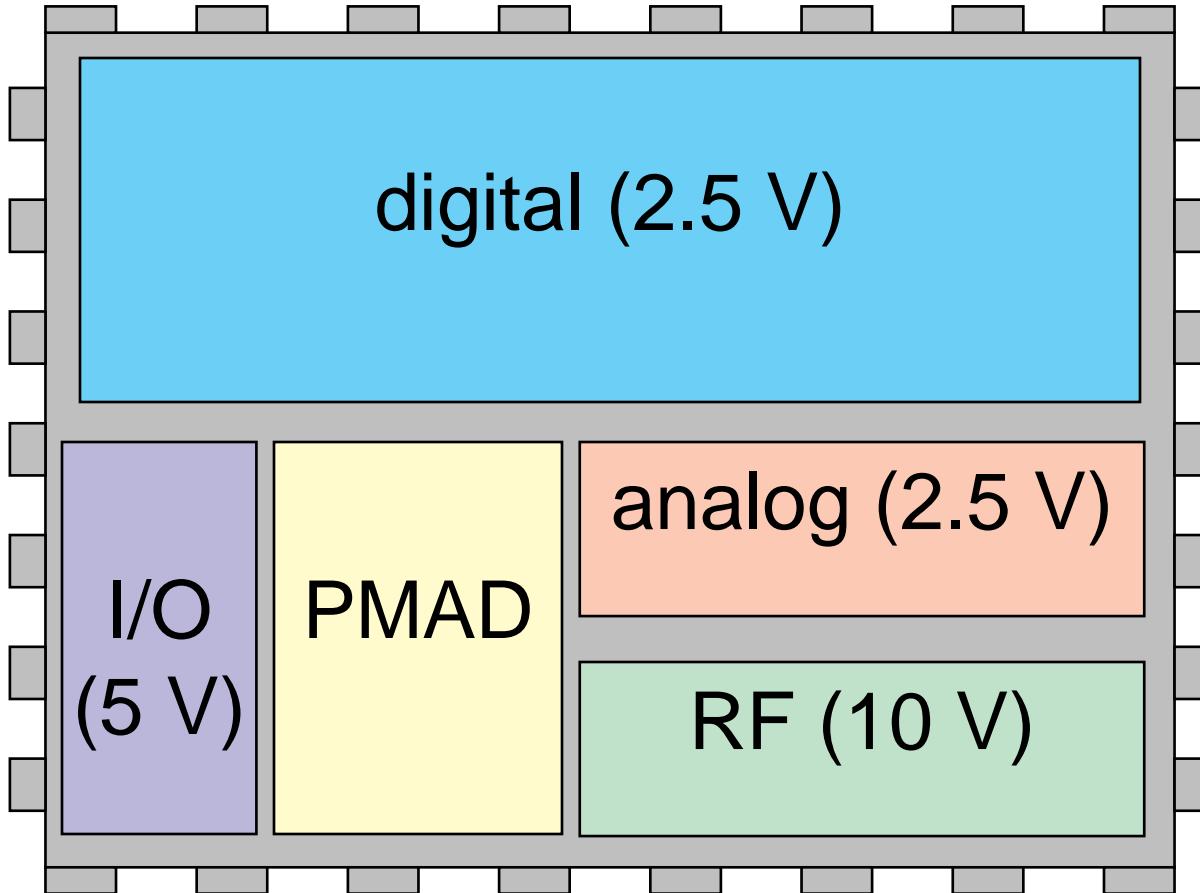
Components

- mixers
- filters
- low-noise amplifier (LNA)
- power amplifier (PA)
- baseband amplifier (BBA)
- intermediate frequency amplifier (IFA)
- voltage-controlled oscillator (VCO)

Frequency Allocation

- 900 MHz - 1.2 GHz
cellular, narrowband PCS
- 1.8 GHz - 2 GHz
broadband PCS

Power Management, Distribution, Regulation, and Conversion



Components

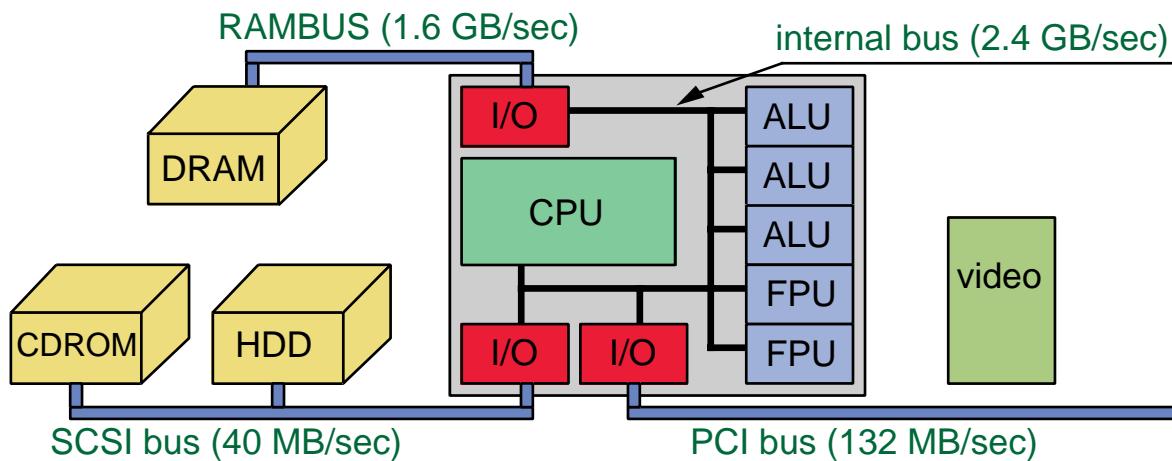
- step-down converter
- step-up converter
- mixed-signal feedback control
- passive components

Issues

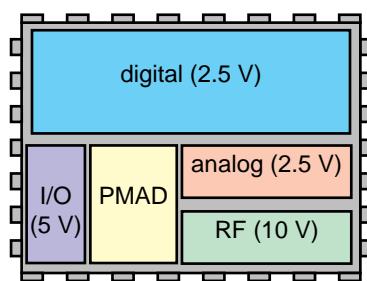
- regulated voltage
- allowable ripple
- load current
- passive component values
- switching frequency
- isolated supply voltages



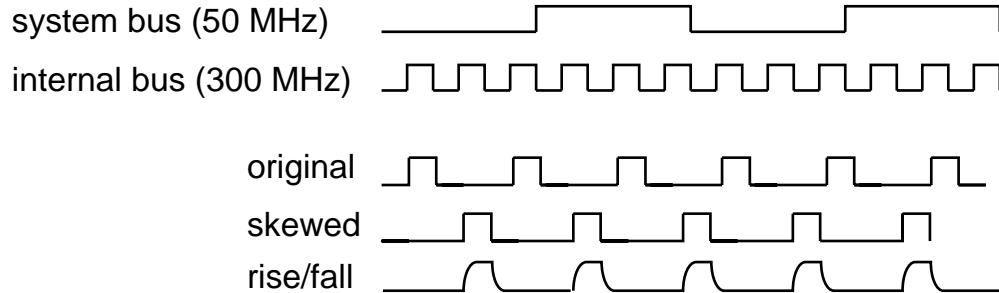
System Architecture and Issues



- bandwidth limited
- need for functional integration

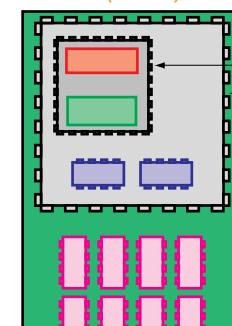


- distributed power supplies
- internal clock distribution
- memory organization



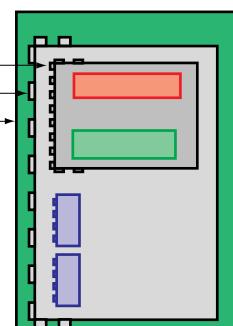
Current Organization

- registers (128 bytes)
- level 1 cache (16 KB)
- level 2 cache (1 MB)
- RAM (32 MB)
- HDD (4 GB)



Future Organization

- registers (256 bytes)
- level 1 RAM (2 MB)
- level 2 RAM (128 MB)
- HDD (16 GB)



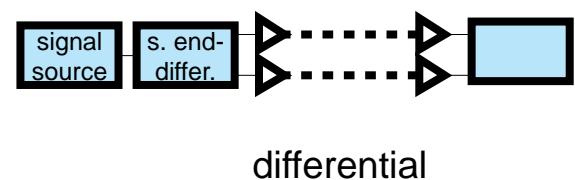
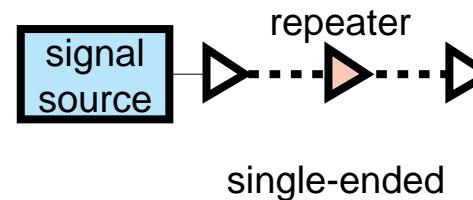
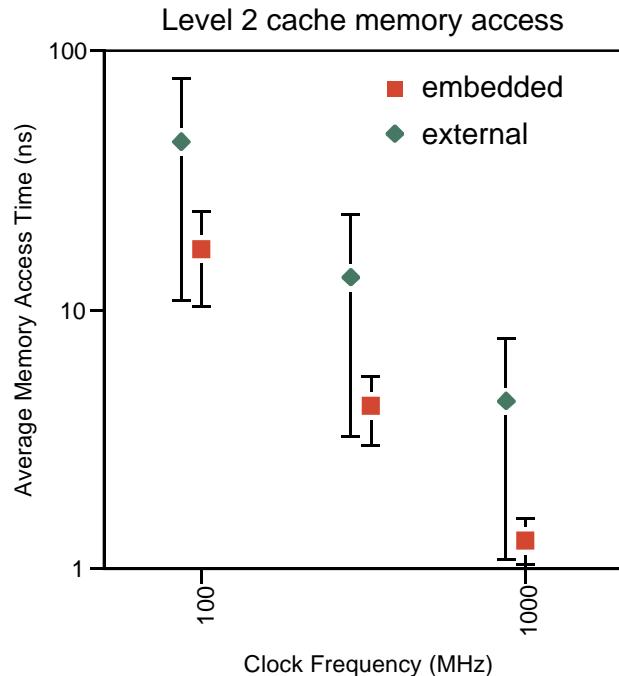
On-Chip Bus Topologies

$$t_{\text{external}} = DC_i + LC_s$$

$$C_s = \frac{C_i}{R}$$

$$t_{\text{embedded}} = DC_i + LC$$

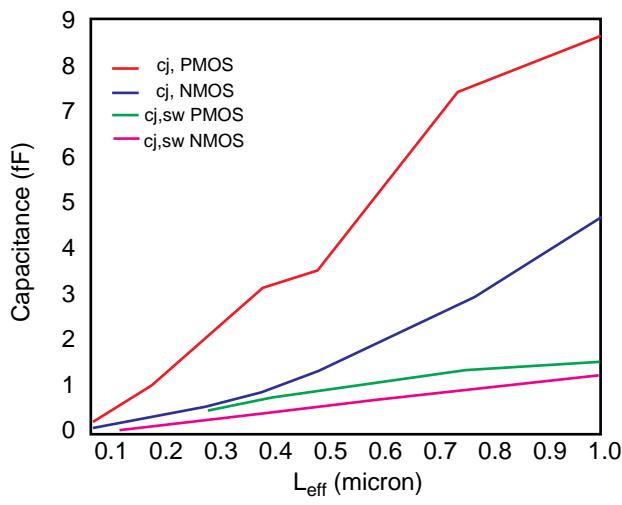
- more accurate physical effects must be introduced
- physical implementation estimation is necessary
- embedded memory has greatly reduced access times
- bounds on memory access time are tighter for embedded memory
- need to place blocks on-chip for high-speed memory access
- direct differential busing to memory differential sensing



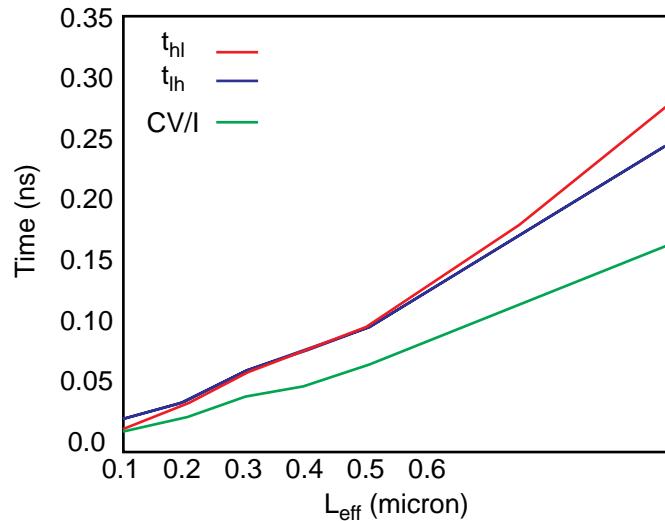


Modeling Metrics

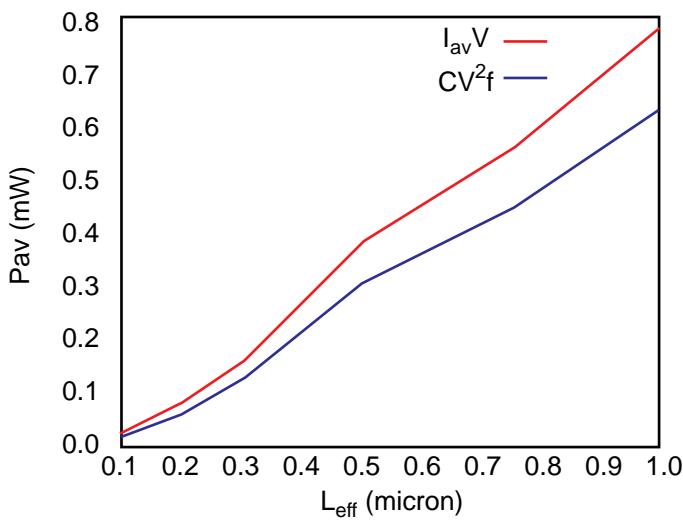
Capacitances



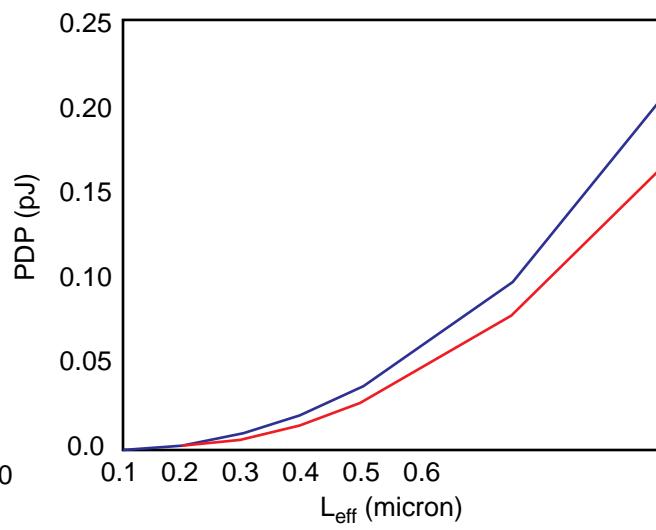
Delay



Power



Power x Delay



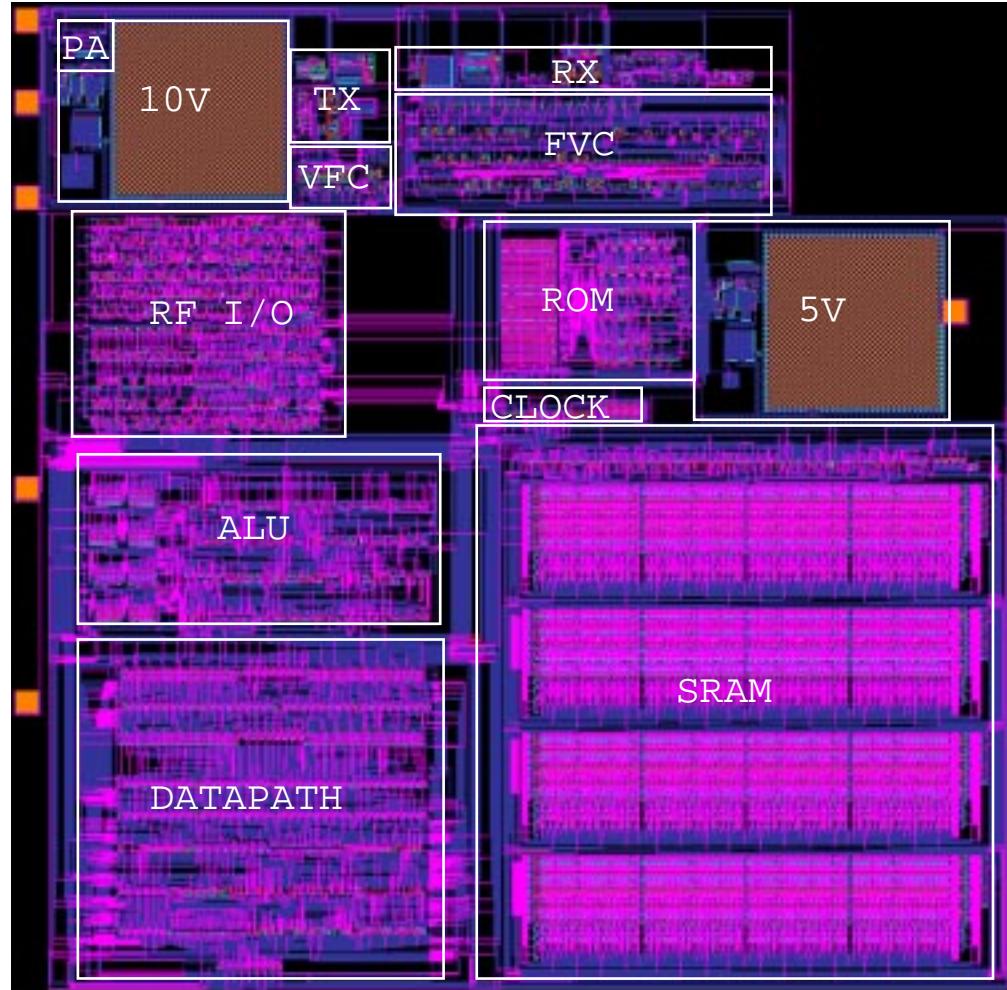
System on a Chip: The UIC Chip

Architecture

- 50 MHz, 8-bit RISC CPU
- 256-byte SRAM
- RF I/O control
- 400 MHz transceiver
- (2) on-chip power regulation and management units
- on-chip clock generation

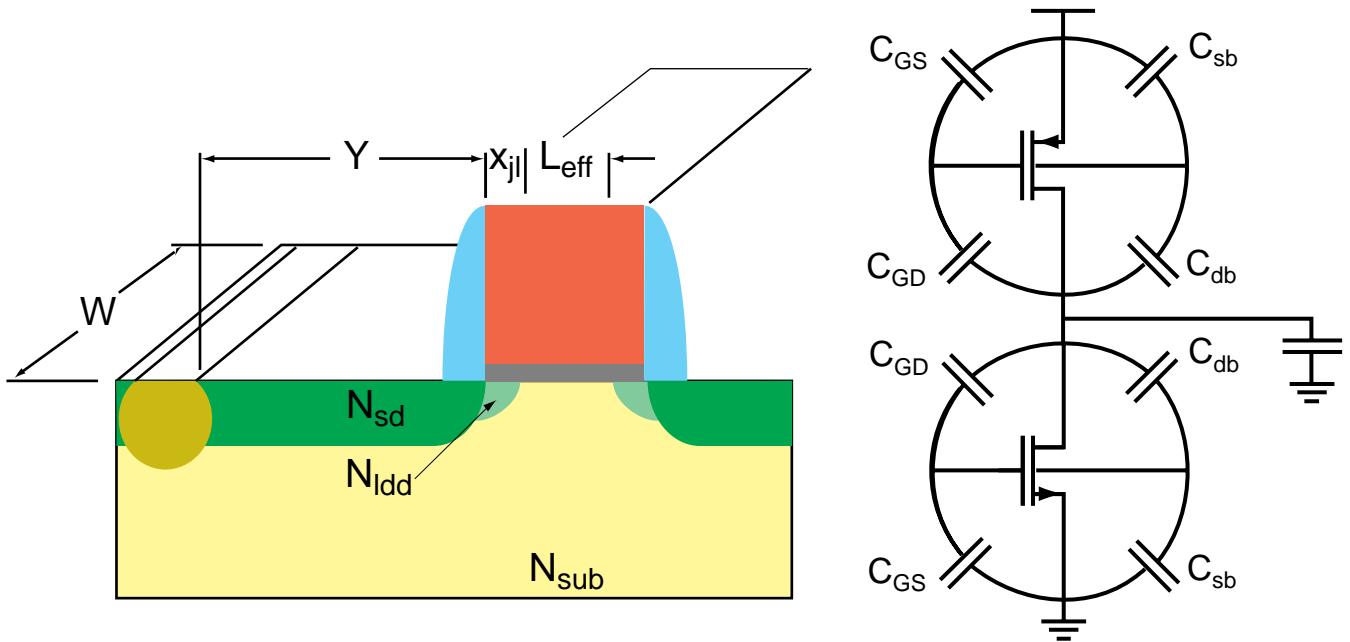
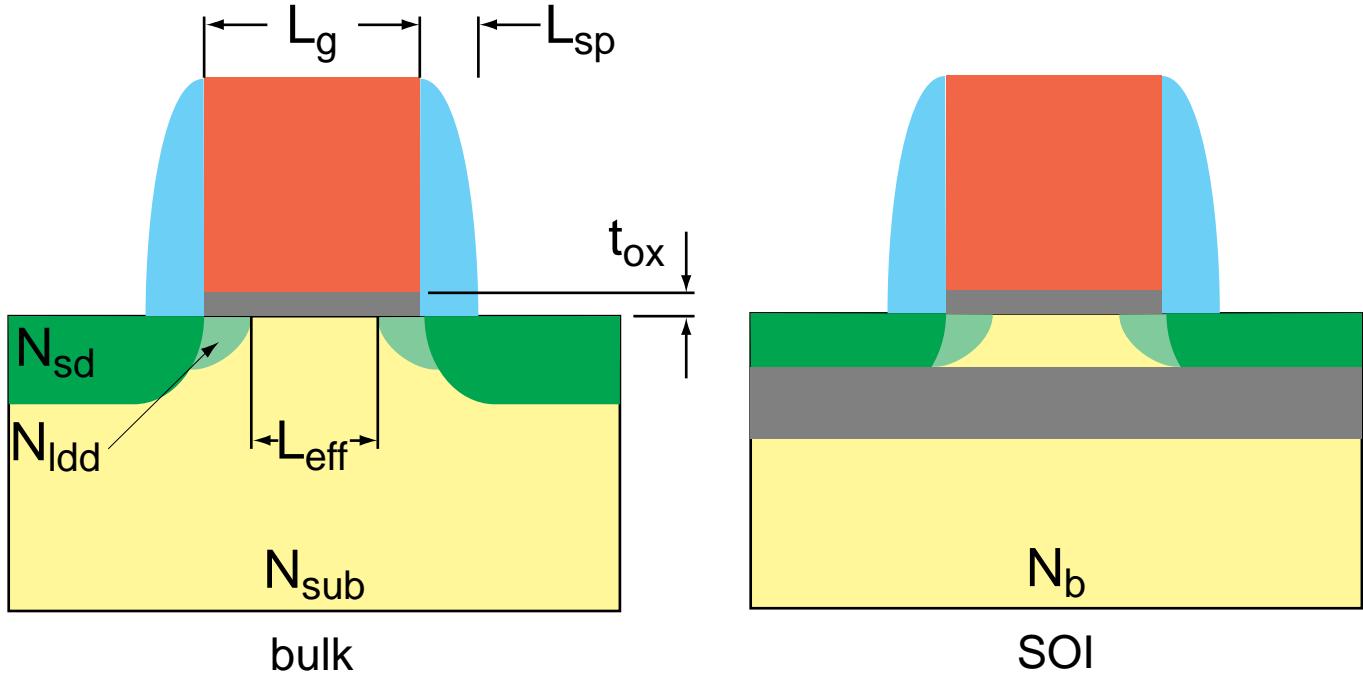
Technology

- 1.2 μ m bulk n-well CMOS
- single poly, dual metal
- MOSIS AMI process



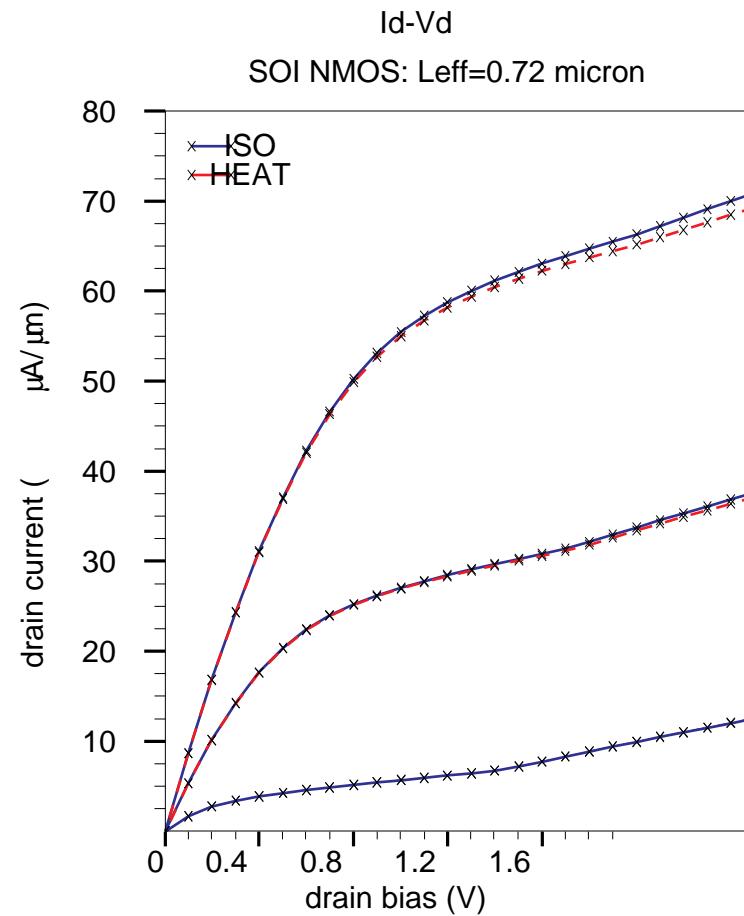
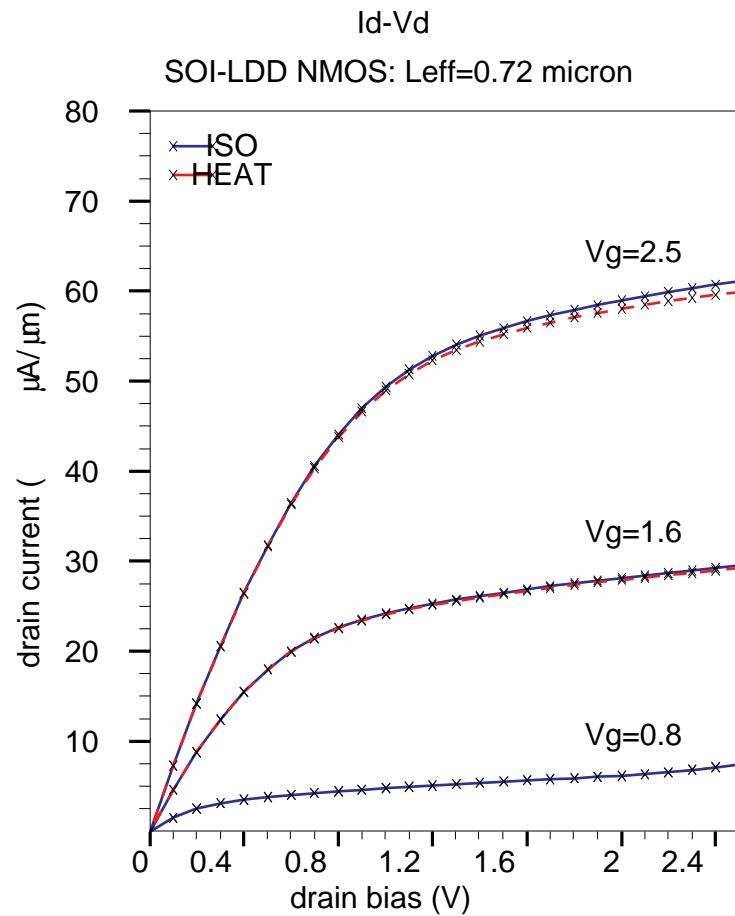


Device Structures





Fully-Depleted SOI Optimization

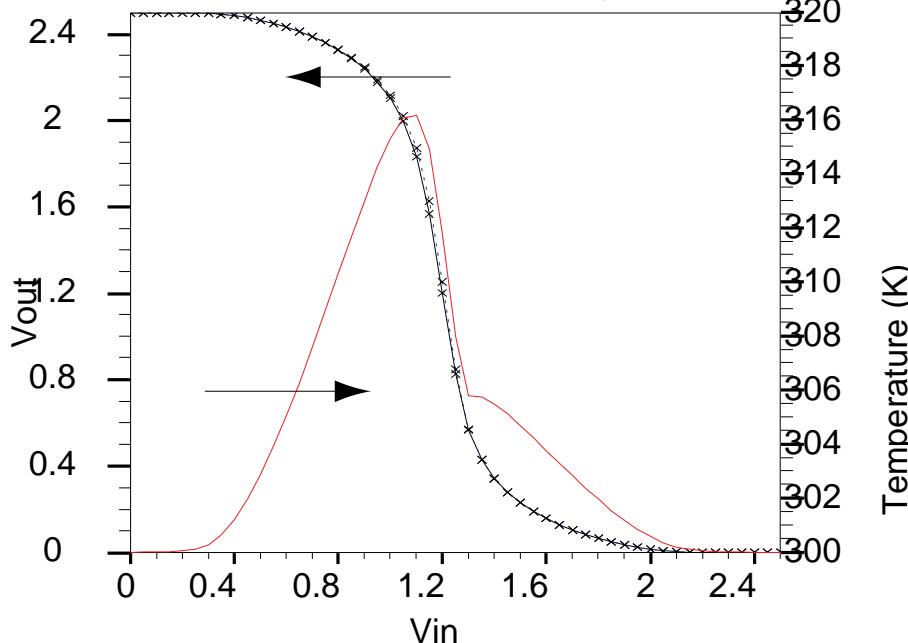


- "kink" effect in plain SOI device not expected in FD SOI
- SOI with LDD shows more optimal performance
 - reduction in drain-body impact generation of carriers
 - no parasitic bipolar or body-source diode action

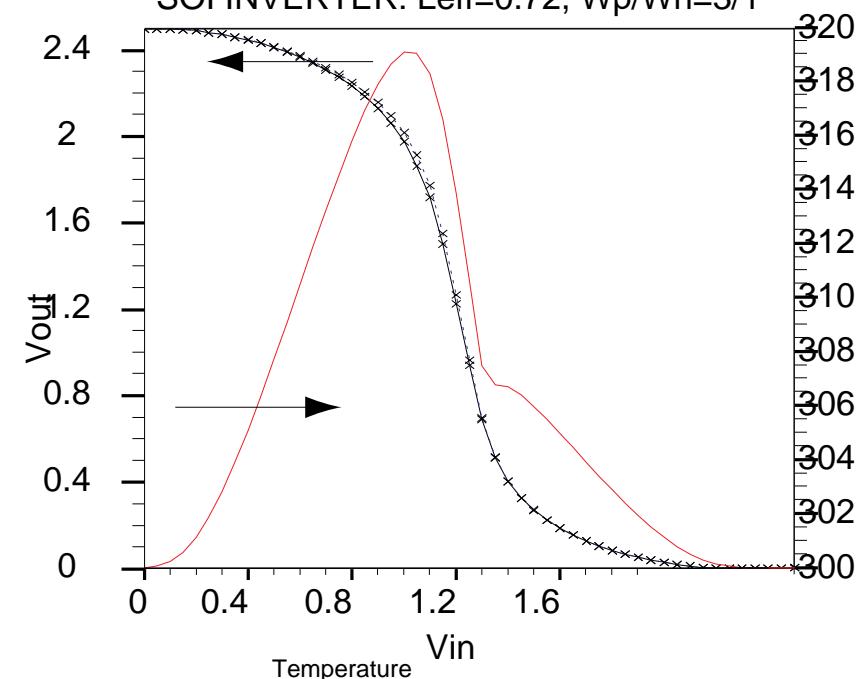


Thermal Effects

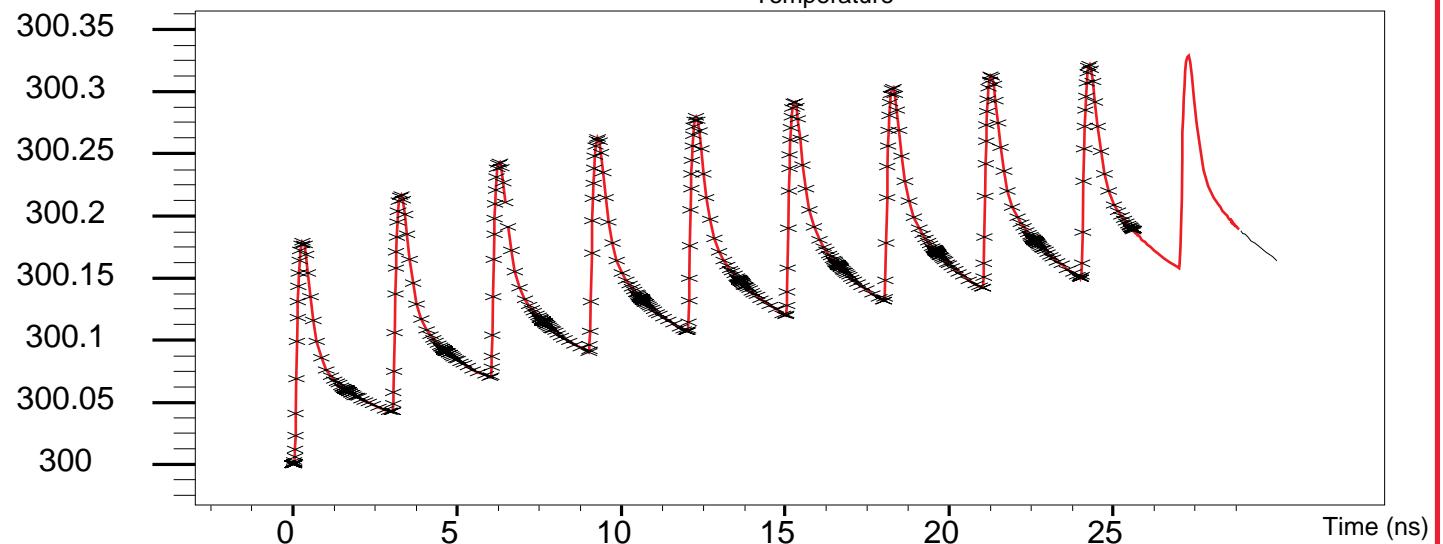
SOI-LDD INVERTER: $L_{eff}=0.72$, $W_p/W_n=3/1$



SOI INVERTER: $L_{eff}=0.72$, $W_p/W_n=3/1$

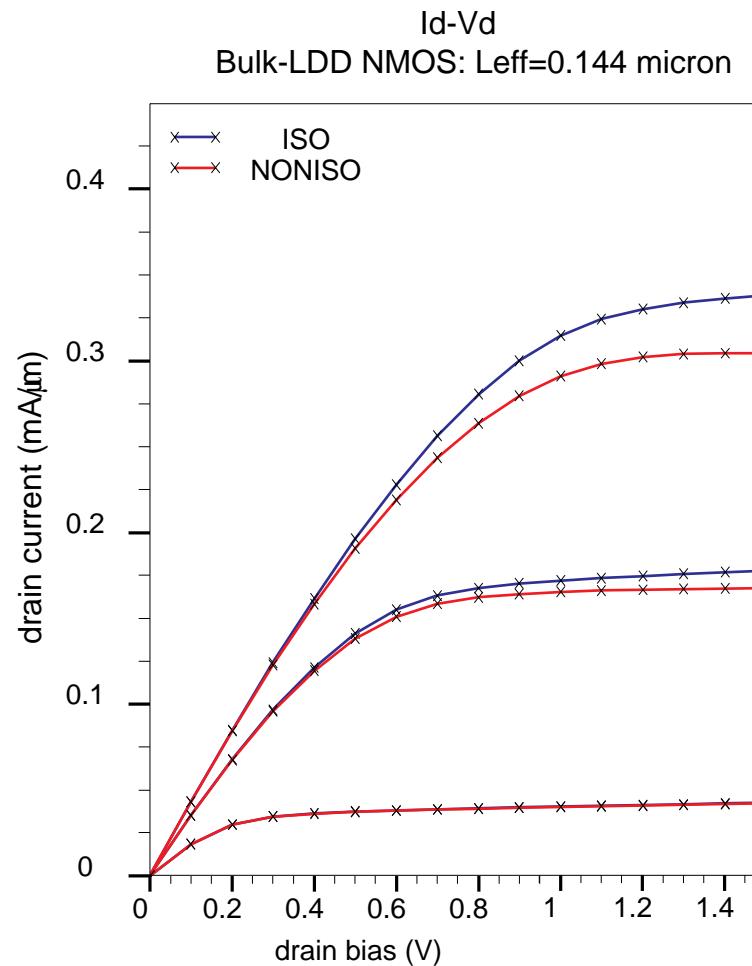
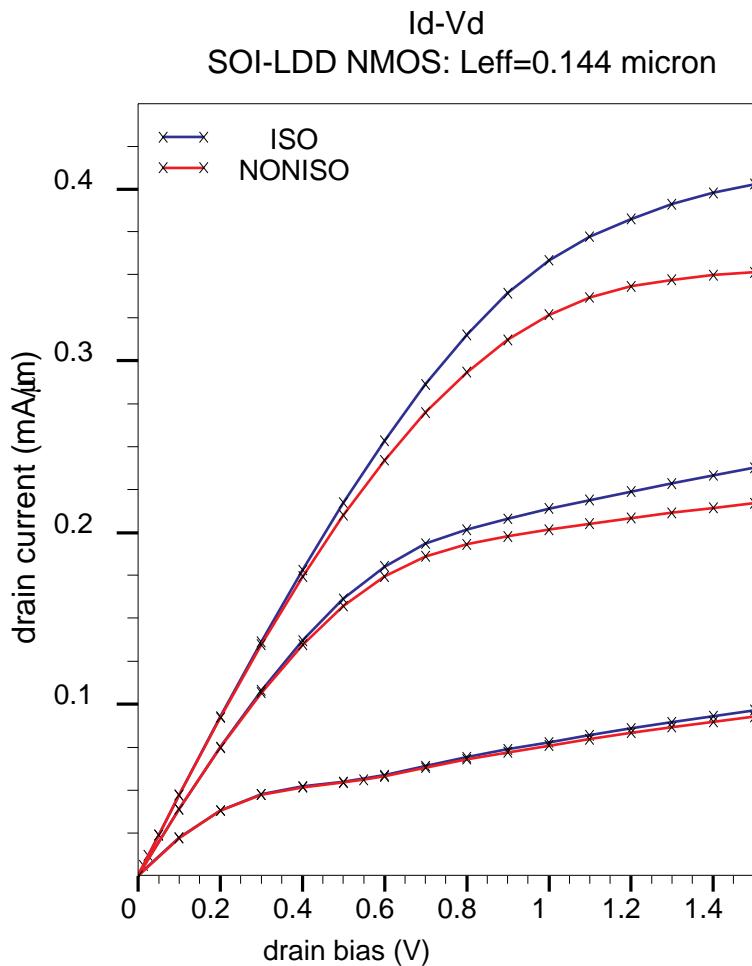


SOI-LDD INVERTER
 $L_{eff}=0.72$, $W_p/W_n=3/1$





Submicron Fully-Depleted SOI Optimization



- suppression of "kink" effect in SOI device requires LDD structure
- significant heating effects compared to bulk device
 - degradation of current density
 - onset of negative differential resistance

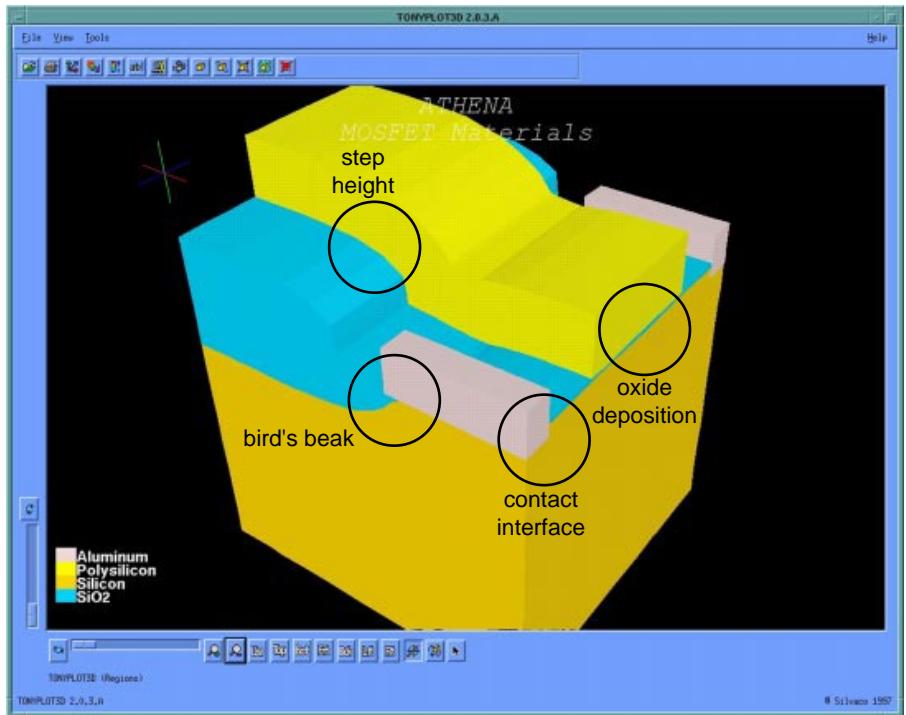


Virtual Reality in Design and Collaboration

Electronic Visualization Laboratory (EVL)
ImmersaDesk



3-D Device Visualization



- electronic visualization for research and education
- integrate VR with EDA tools
- real-time interaction with test equipment
- visualization and prototyping testbed

KRISHNA SHENAI.

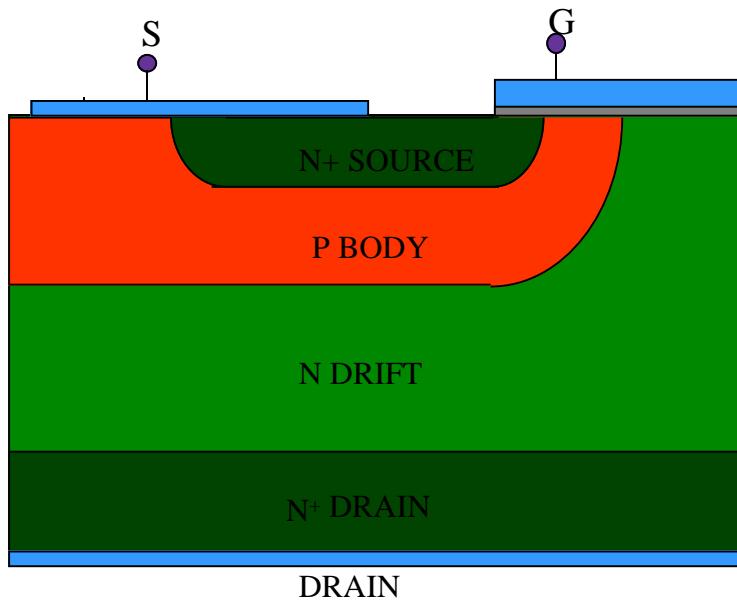


RF ISSUES

- Static Characteristics
 - Output Characteristics
 - Transconductance
- Capacitance
- S-Parameters
- P_{IN} - P_{OUT} /Efficiency
- Linearity
- Distortion
- Noise

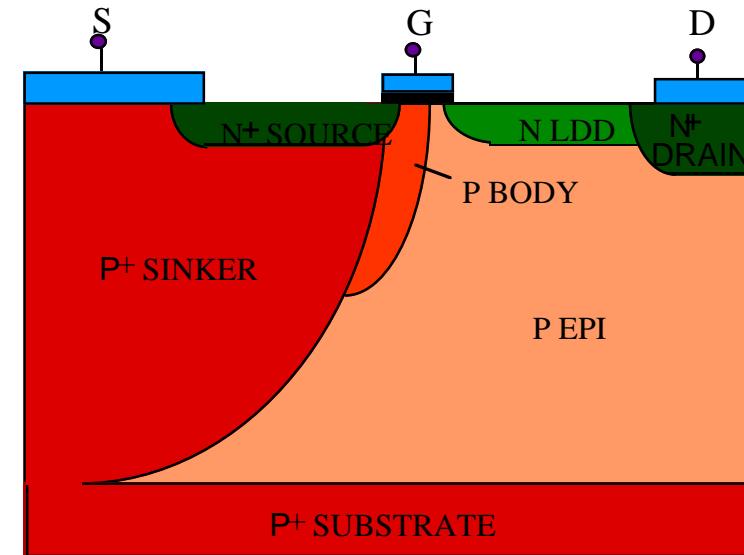
- Thermal Issues
- De-embedding
- Packaging Parasitics

POWER MOSFETs FOR RF APPLICATIONS



Vertical DMOSFET (VDMOS)

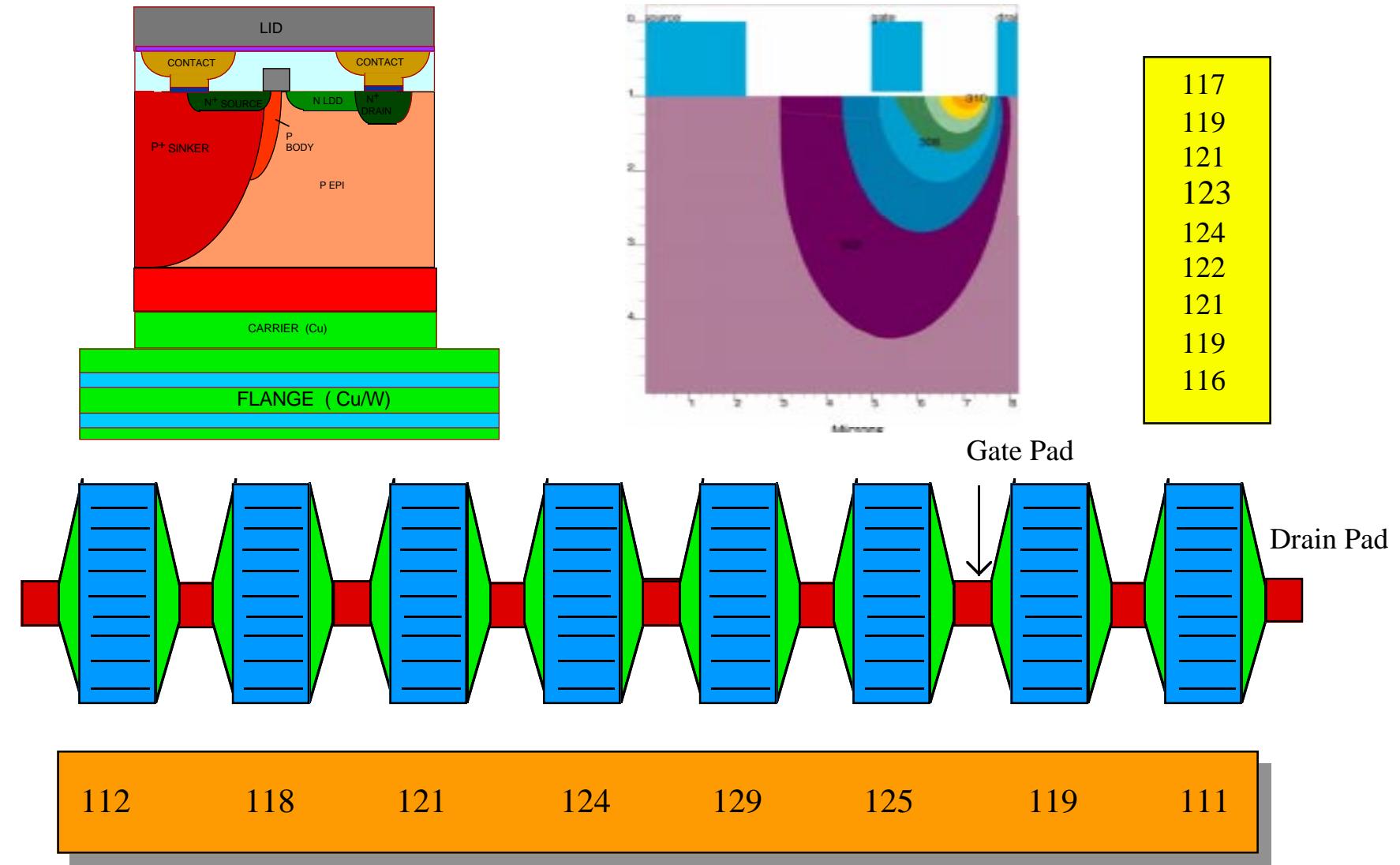
- High Packing Density
- Large C_{GD}
- Current Crowding



Lateral DMOSFET (LDMOS)

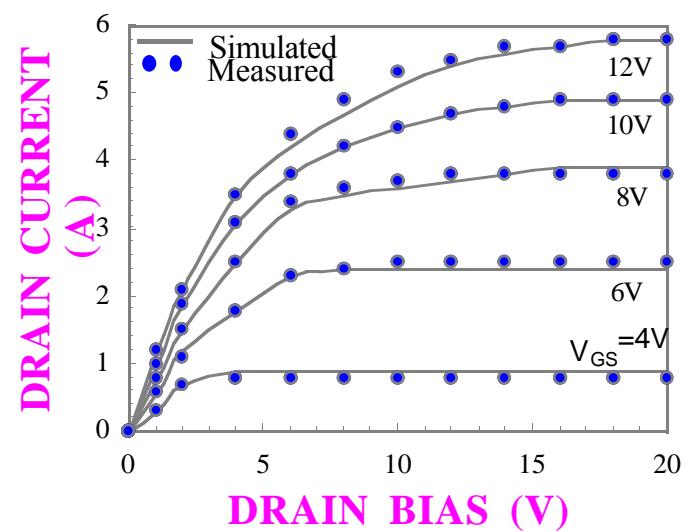
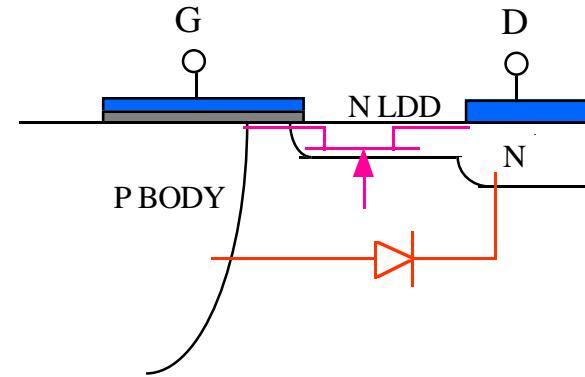
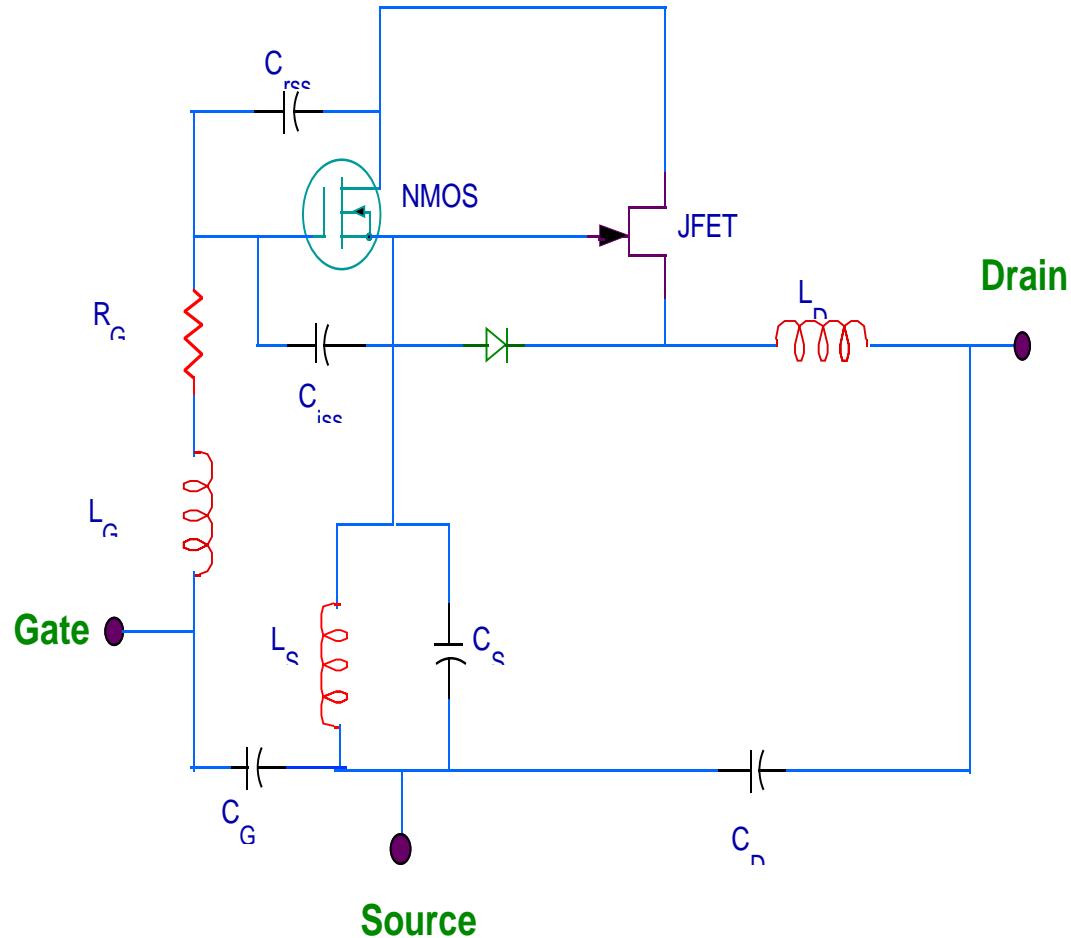
- Easier Integration
- Lower C_{GD}
- Low Packing Density

TEMPERATURE VARIATIONS

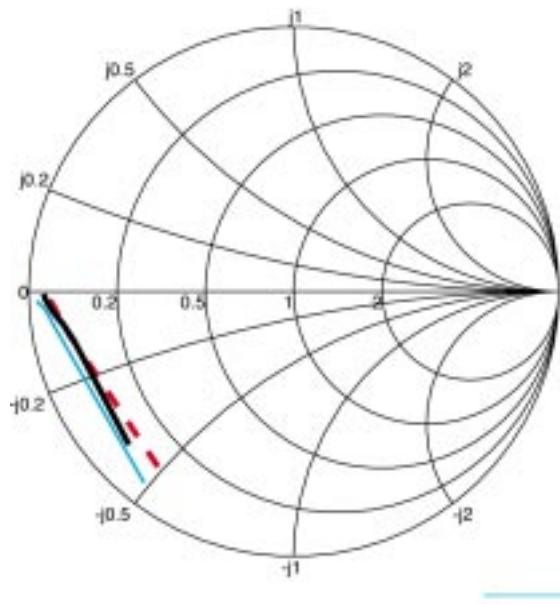
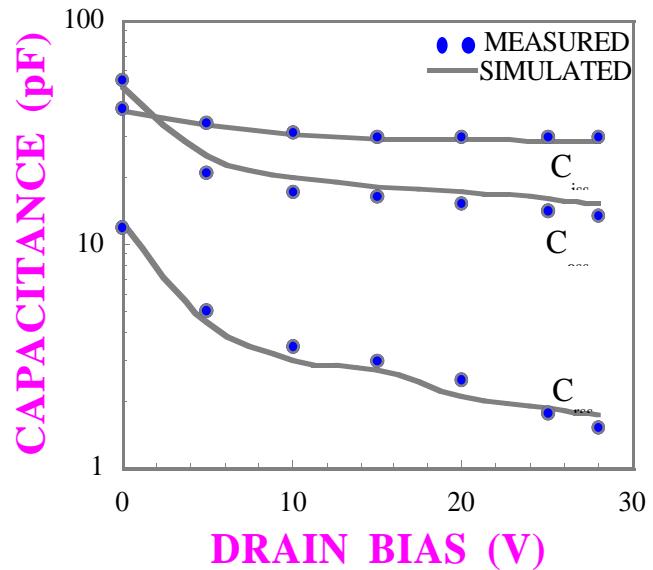
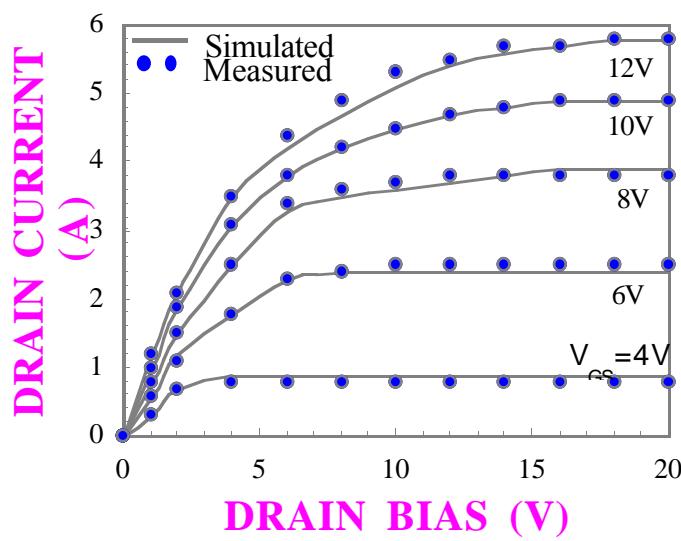




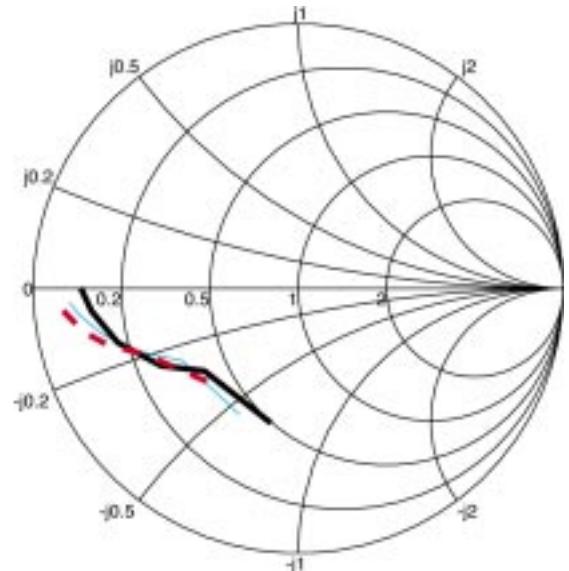
CIRCUIT MODEL FOR LDMOSFET



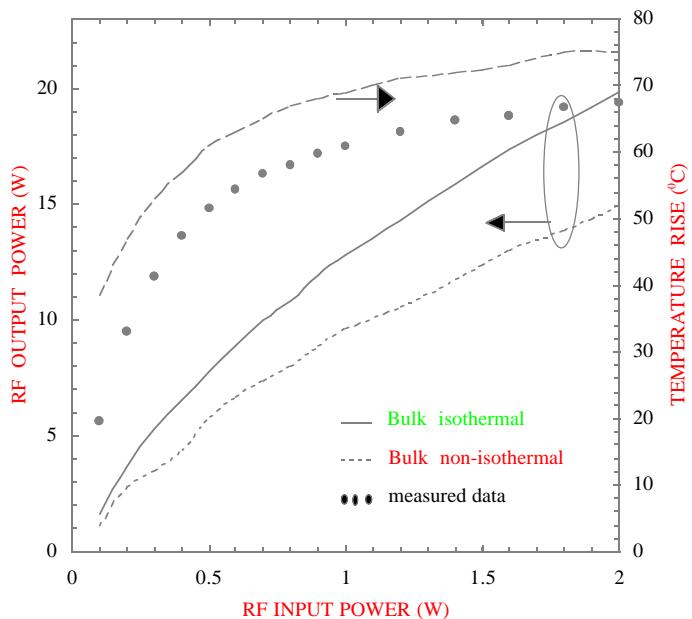
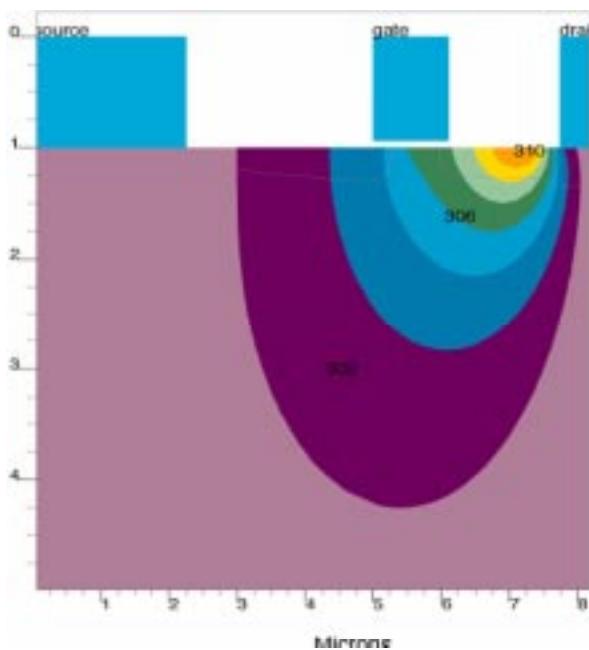
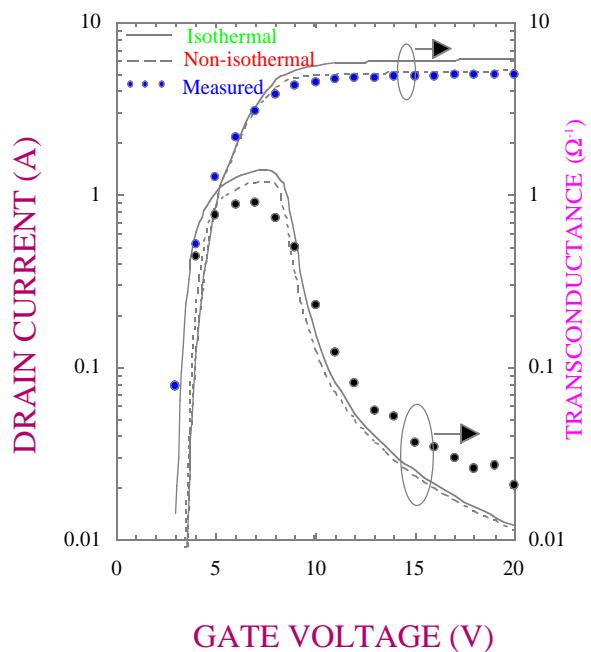
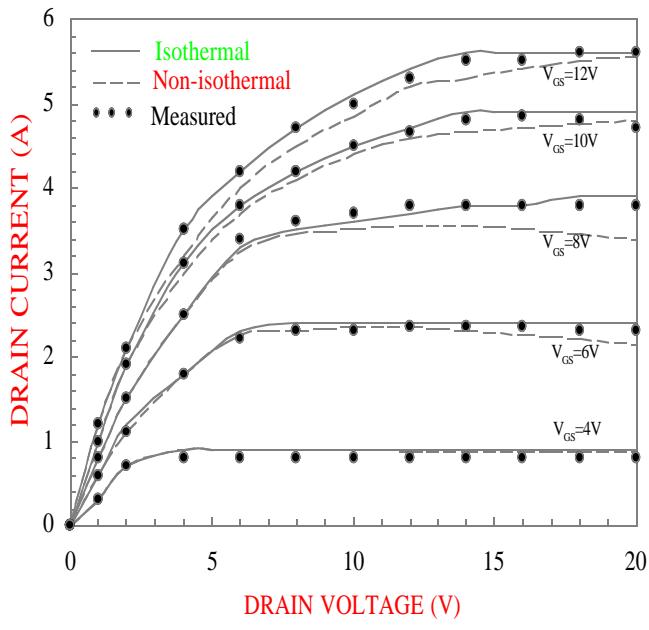
2-D SIMULATIONS



SIMULATED
MODELED
MEASURED



MEASUREMENTS & SIMULATIONS

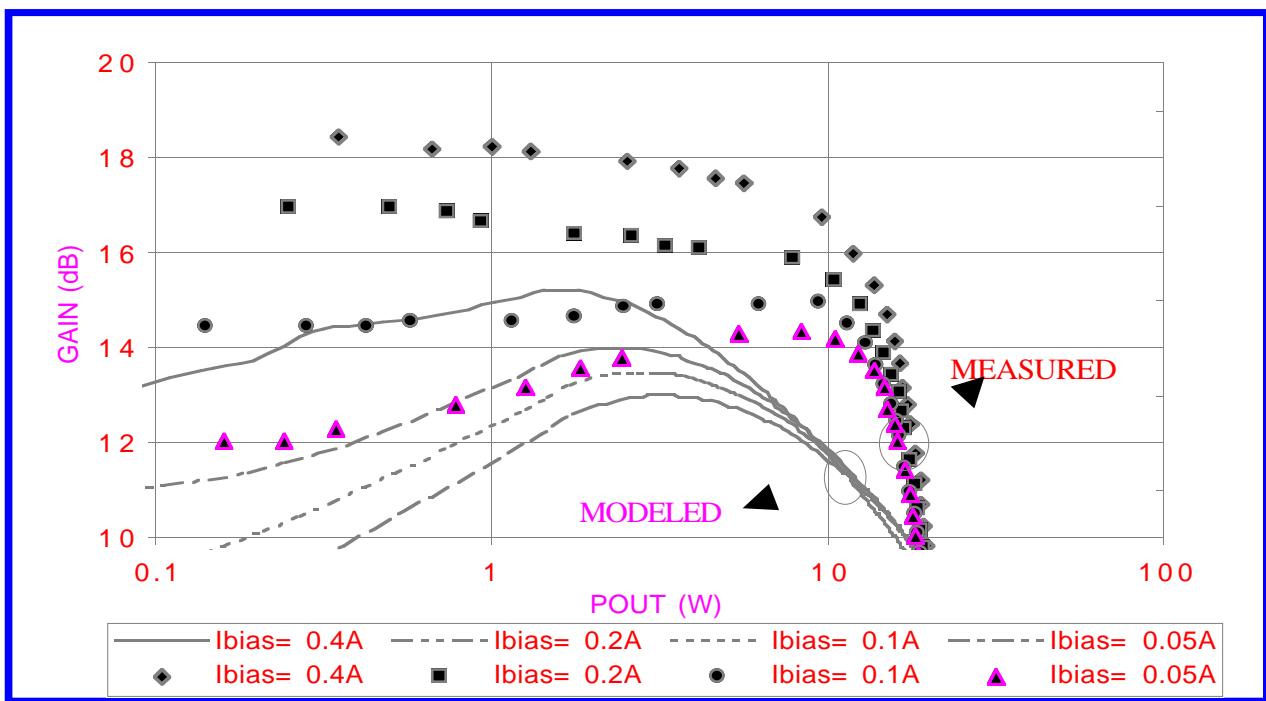
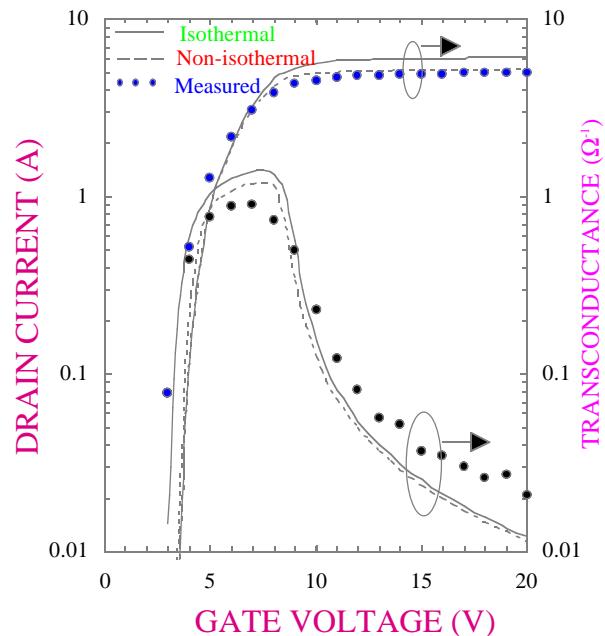


LINEARITY & P_{IN}-P_{OUT}

$$g_m = \frac{\mu_0 C_{ox} W}{\left(1 + \frac{\mu_0 (V_{GS} - V_T)}{L v_{sat}}\right) L} (V_{GS} - V_T) \quad \text{MOS Saturation & Velocity Saturation Region}$$

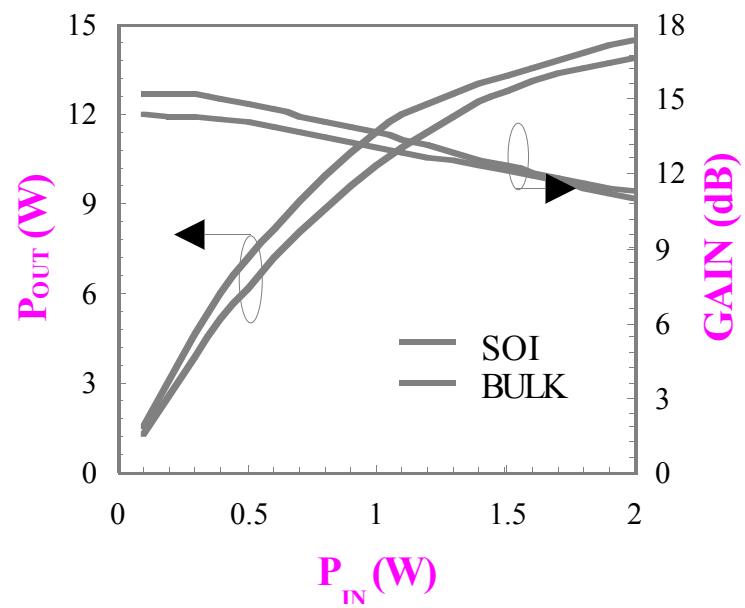
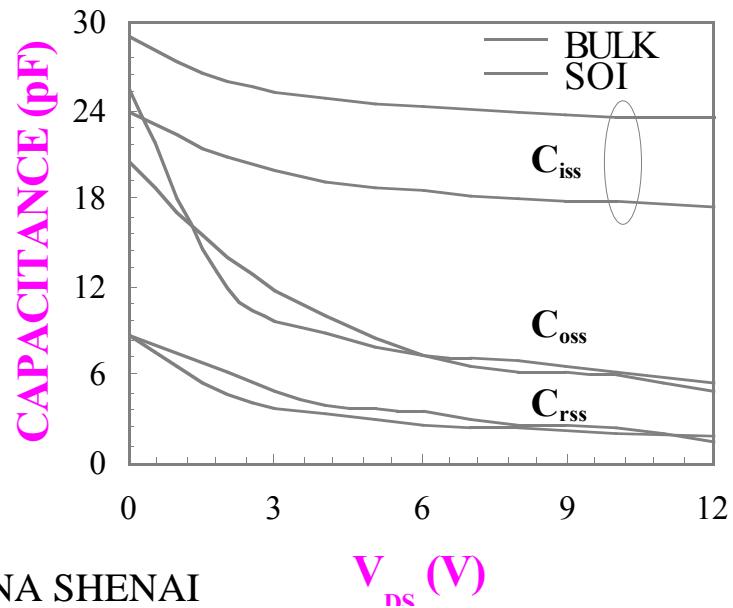
$$= \frac{\mu_0 C_{ox} W / L V_{DS,m}}{\left(1 + \frac{\mu_0 (V_{GS} - V_T)}{L v_{sat}}\right) + \frac{\mu_0 C_{ox} W (V_{GS} - V_T - V_{DS,m})}{2 L \sqrt{\beta I_{DS}}}} \quad \text{JFET Saturation}$$

$$GAIN = \frac{g_m^2 R_L}{\omega^2 \left[C_{iss} + C_{rss} \left(1 + \frac{g_m}{g_{m,j}}\right)^2 \right] R_G \left(1 + \omega^2 C_{oss}^2 R_L^2\right)}$$



COMPARISON OF RF PERFORMANCE

PARAMETER	BULK	SOI
V_{BD}	49	49
Specific On-Resistance ($\text{m}\Omega\text{cm}^2$)	1.06	0.50
$g_m (\Omega^{-1})$ at $V_{DS}=12\text{V}$	1.48	1.75
C_{iss} (pF) at $V_{DS}=12\text{V}$	23.5	17.5
C_{rss} (pF) at $V_{DS}=12\text{V}$	1.9	1.6
Power Gain (dB)	7.85	9.52
Noise Figure (dB)	7.1	6.91

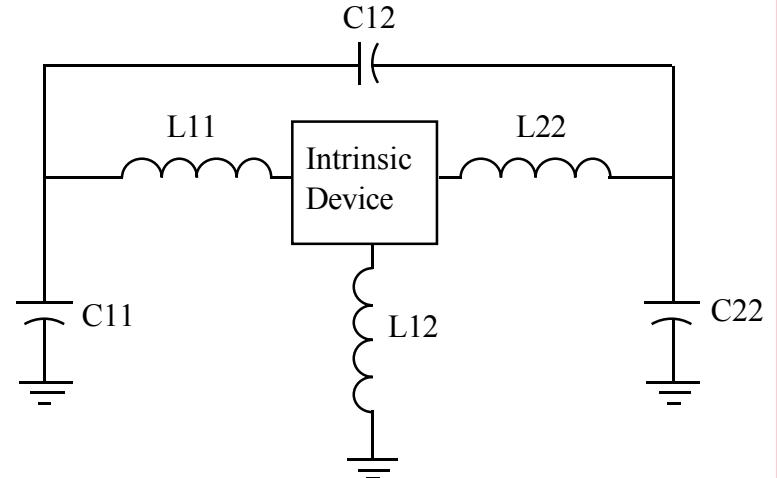




PARASITIC DE-EMBEDDING TECHNIQUES

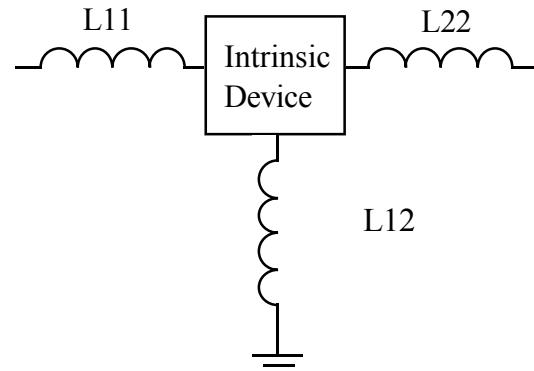
Multiple Parasitic Layers

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$



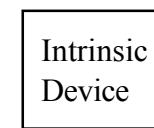
Convert S to Y

$$\begin{bmatrix} Y_{11} - j\omega(C_{11} + C_{12}) & Y_{12} - j\omega C_{12} \\ Y_{21} - j\omega C_{12} & Y_{22} - j\omega(C_{12} + C_{22}) \end{bmatrix}$$



Convert Y to Z

$$\begin{bmatrix} Z_{11} - j\omega(L_{11} + L_{12}) & Z_{12} - j\omega L_{12} \\ Z_{21} - j\omega L_{12} & Z_{22} - j\omega(L_{12} + L_{22}) \end{bmatrix}$$





WORK IN PROGRESS

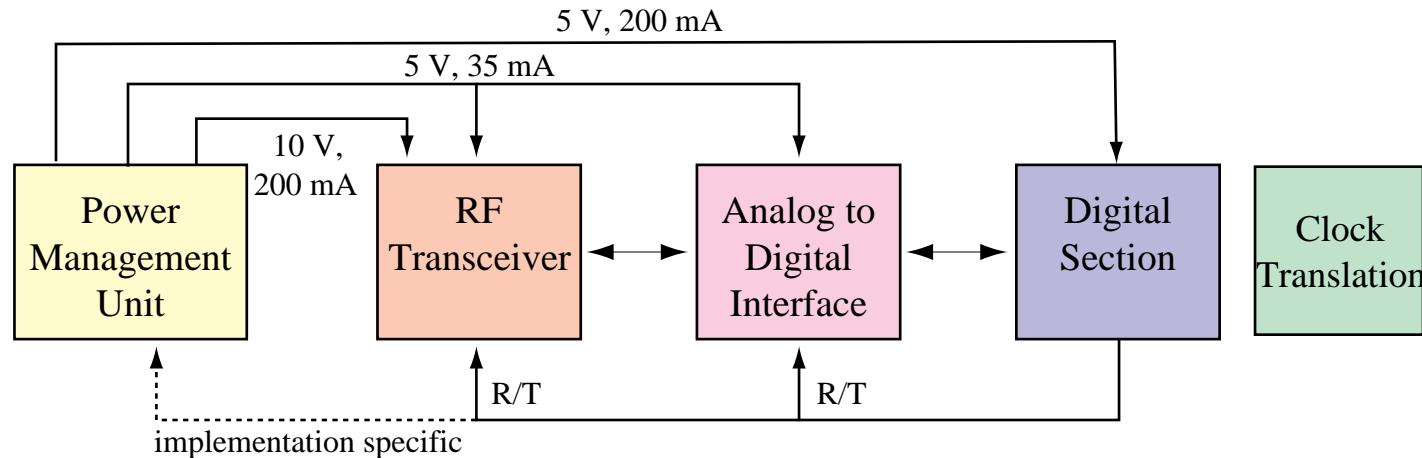
- Bias Dependent Capacitance Modeling
- Linearity, Distortion & Noise Issues
- Improved Device Structures
 - Bulk Substrates
 - SOI Substrates
 1. Thick Film SOI
 2. Thin Film SOI (RESURF)
- Optimized Cell Layout
- Package Design & Modeling

On-Chip Power Generation and Distribution for RF Applications

- Circuit Topology
 - DC/DC Converters
- Component Modeling
 - Power Components
 - Passive Components
- Miniaturized Magnetics
- Fabrication Technology
 - All CMOS
- Typical Applications



RF and Power Architecture



- power conversion from 5 V supply to 5V/10V with 5% ripple
- power management includes sleep mode to power-down 10 V supply when not used for RF transceiver
- clock converter, 400 MHz \rightarrow 50 MHz
 - 400 MHz clock for local oscillator
 - crystal for 400 MHz clock is only discrete off-chip component
- on-chip RF transceiver
 - 400 MHz
 - 8 tones transmitted over a 100 kHz bandwidth
- tone converter translates frequency to 0–5 V digital swing

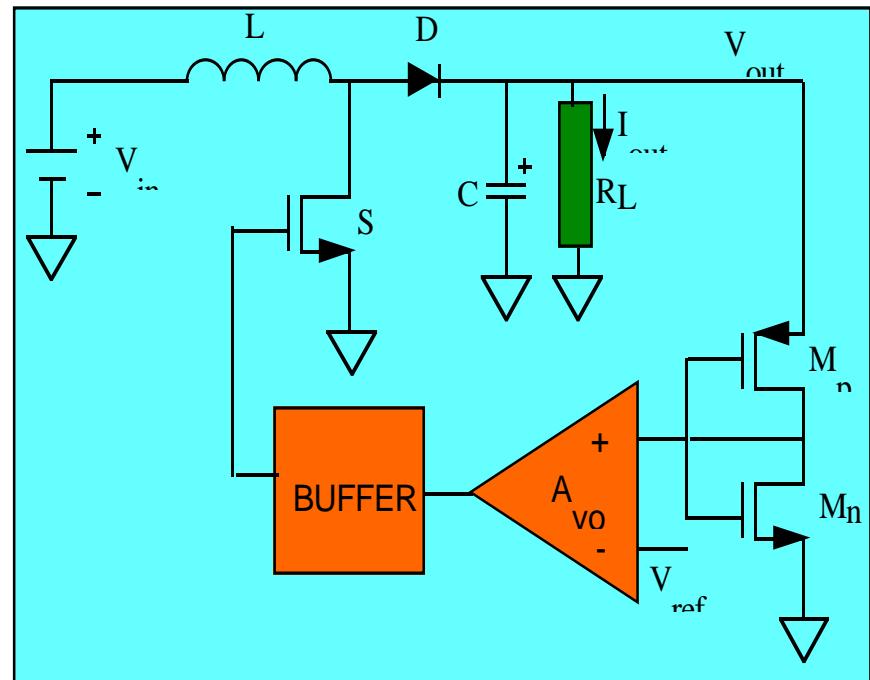
POWER SPECIFICATIONS

- 5 V External Battery, 20% Ripple (4 V-6 V)
- 5 V, 200 mA Supply for Analog and Digital Sections, 5% Ripple (4.75 V - 5.25 V)
- 10 V, 200 mA Supply for Transmitter Power Amplifier, 5% Ripple (9.5 V - 10.5 V)
- $V_{BD} = 14 \text{ V}$ (nMOS), 12 V (pMOS)
- Specific Implementation makes Analog and Digital Isolation Non-Critical, so single Supply can Power Both Sections

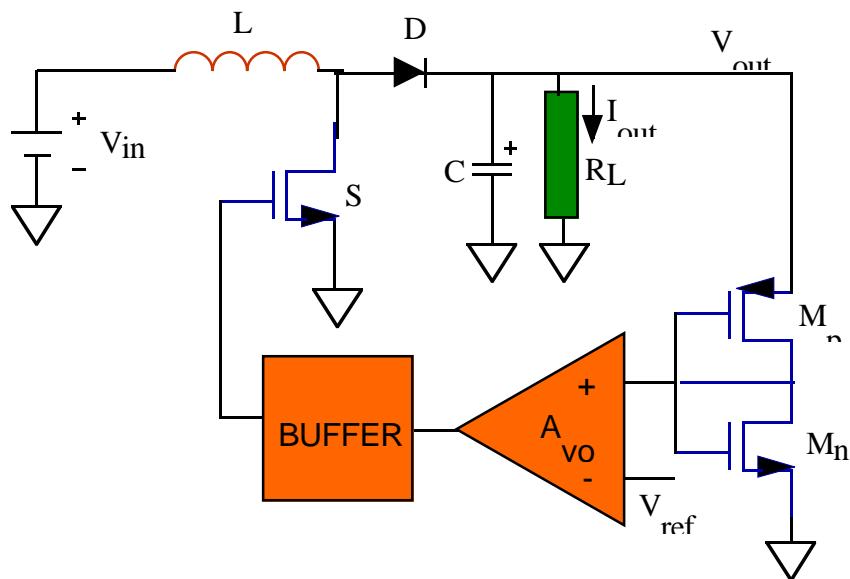
On-Chip DC/DC Converter

Boost Converter

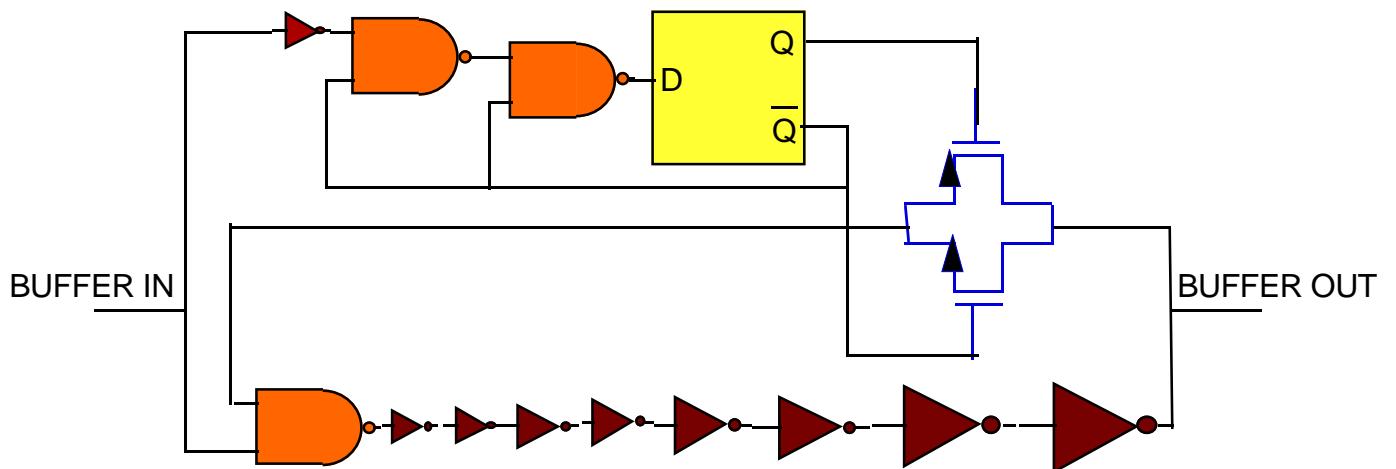
- on-chip implementation
 - $L \sim \text{few nH}$
 - $C \sim 100 \text{ pF}$
 - $f \sim 300 \text{ MHz}$
- Schmidt-trigger feedback for voltage regulation
 - Non-inverting trigger for boost
 - Inverting trigger for buck



PRACTICAL POWER SUPPLY SCHEMATIC



BUFFER



DESIGN PARAMETERS OF POWER SUPPLIES

PARAMETER	(5 V, 35 mA)	(5 V, 200 mA)	(10 V, 200 mA)
V_{OUT}	5.08 V - 5.87 V	5.1 V - 6.6 V	10.02 V - 11.26 V
I_{OUT}	35 mA	200 mA	200 mA
ΔV_{out}	0.12 V-0.83 V	0.4 V - 1.72 V	0.53 V - 1.63 V
R_L	150 Ω	25 Ω	50 Ω
f_s	1 Mhz - 122 MHz	1 Mhz - 127 MHz	1 Mhz - 70 MHz
L	2 nH	7 nH	16 nH
C	1 nF	1 nF	1 nF
W_{GATE}	3400 μ m	3400 μ m	3400 μ m
C_{GATE}	7.5 pF	7.5 pF	7.5 pF

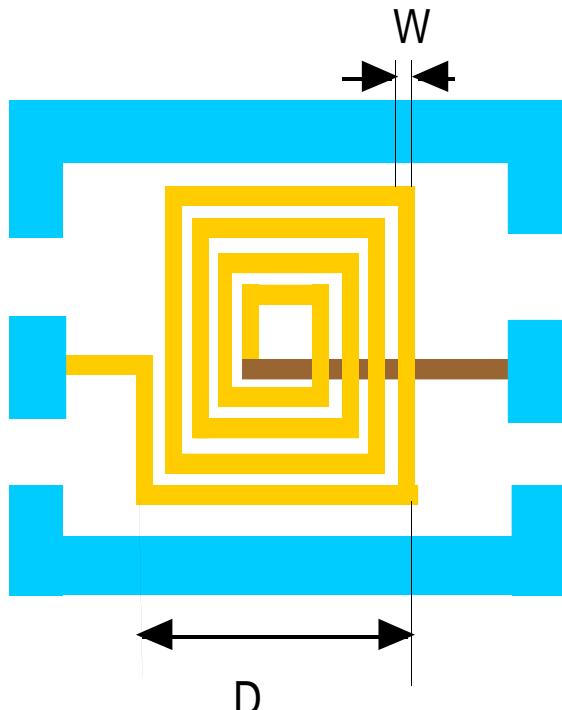
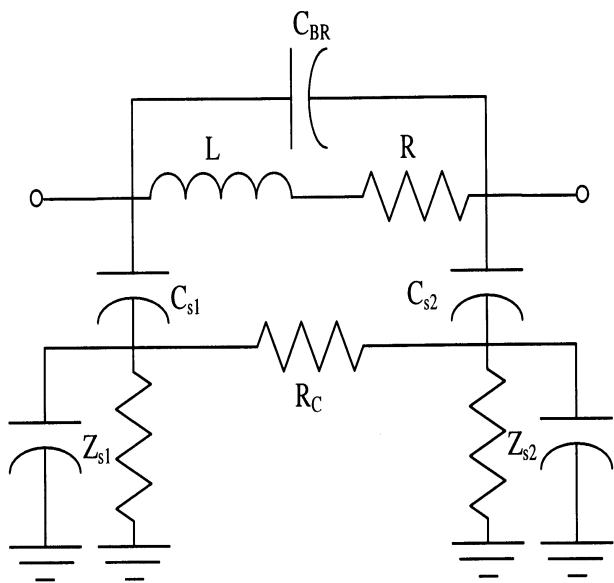
The table reports extreme limits of output voltage swing over the entire span of input voltage and load variations.

The frequency range reported is the maximum swing of the switching frequency over the entire load variation.

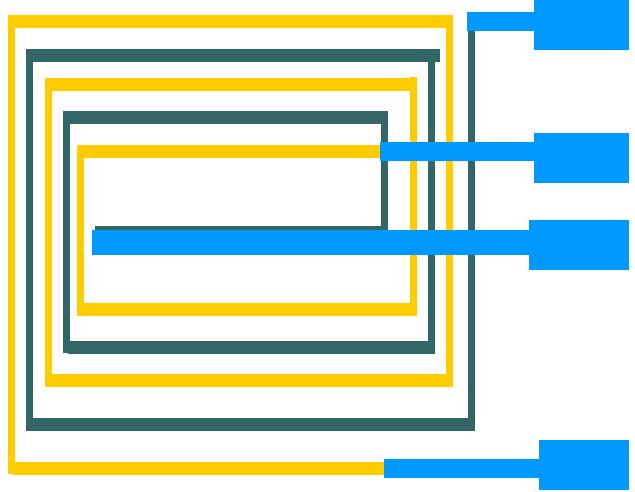
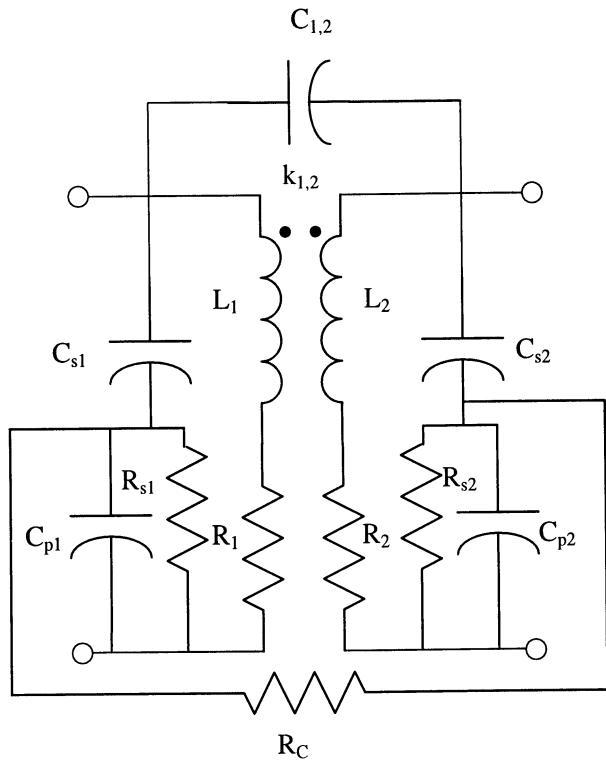


On-chip Passive Components

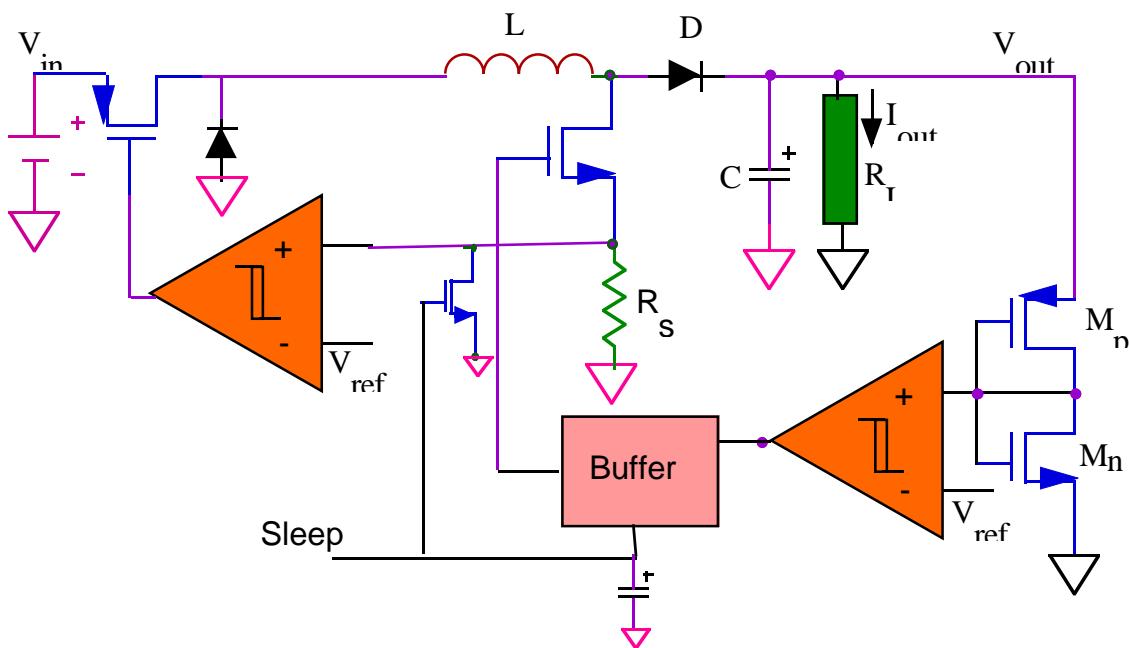
On-chip Inductor



On-chip Transformer



FUTURE WORK

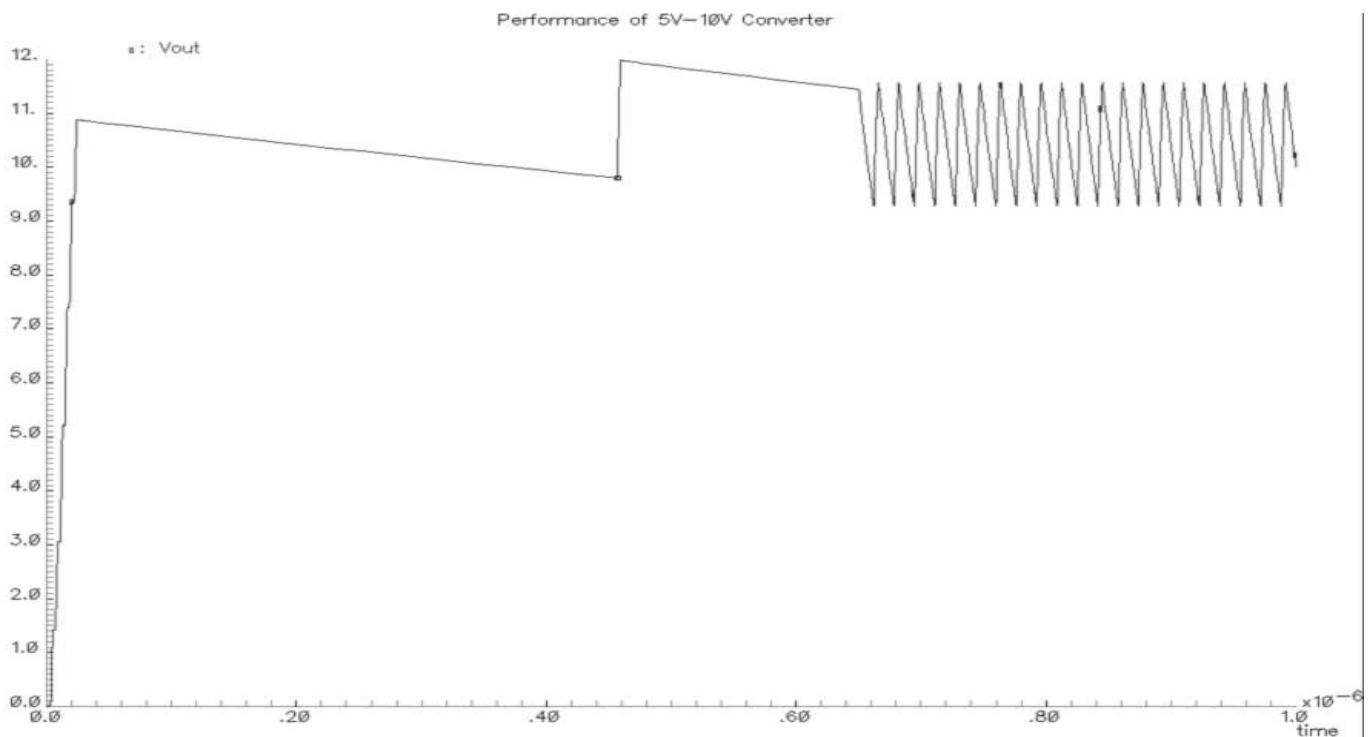


- Inclusion of “Sleep-Mode”
- Desaturation loop for inductor
- Improved efficiency, especially for low load

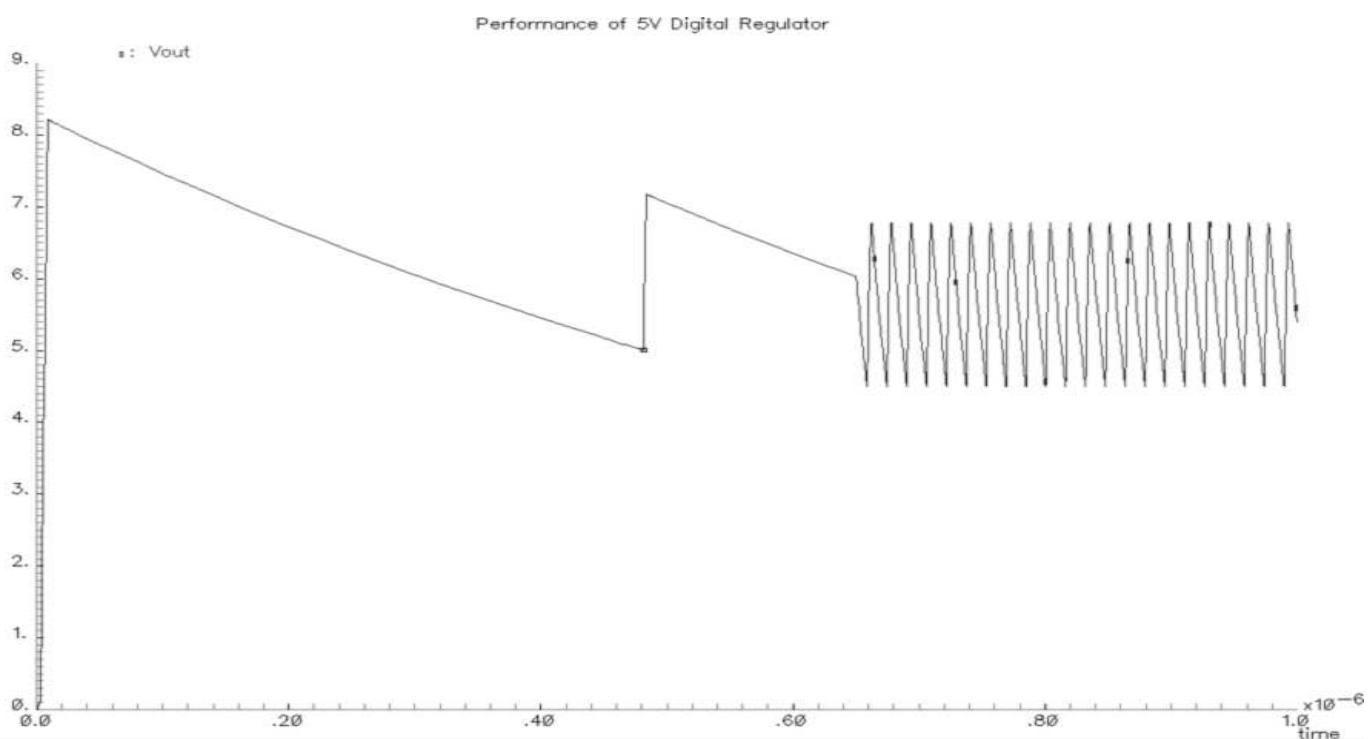


DC-DC Converter Performance

Performance of 5V-10V converter



Performance of 5V digital regulator

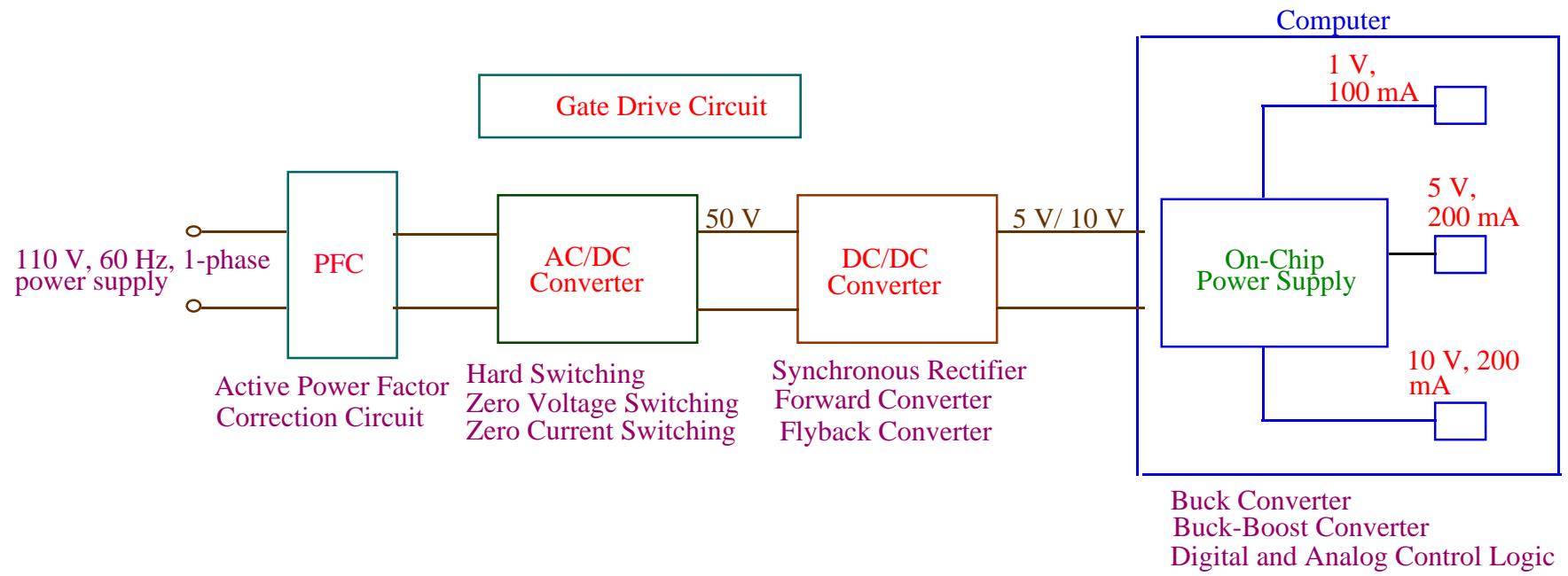




EECS 445: Power Electronic Circuits

- Class Registration: 15
- Tools in Use: Saber, Cadence
- Project: Design of Power Supply for Computer Systems
 - Design of a power electronics circuit that will take input from the ac mains (110 V, 1φ) and supply multiple voltage levels (1 V, 5 V, 10 V) on-chip for computer and multi-media applications.

Power Management And Distribution For Computer Power Supply (Class Project : EECS-445)



- Evaluation of different switching topologies for AC/DC and DC/DC Converter
- Implementation of Active Power Factor Correction circuit
- Logic control and Analog Circuit design for the regulation of on-chip power supply

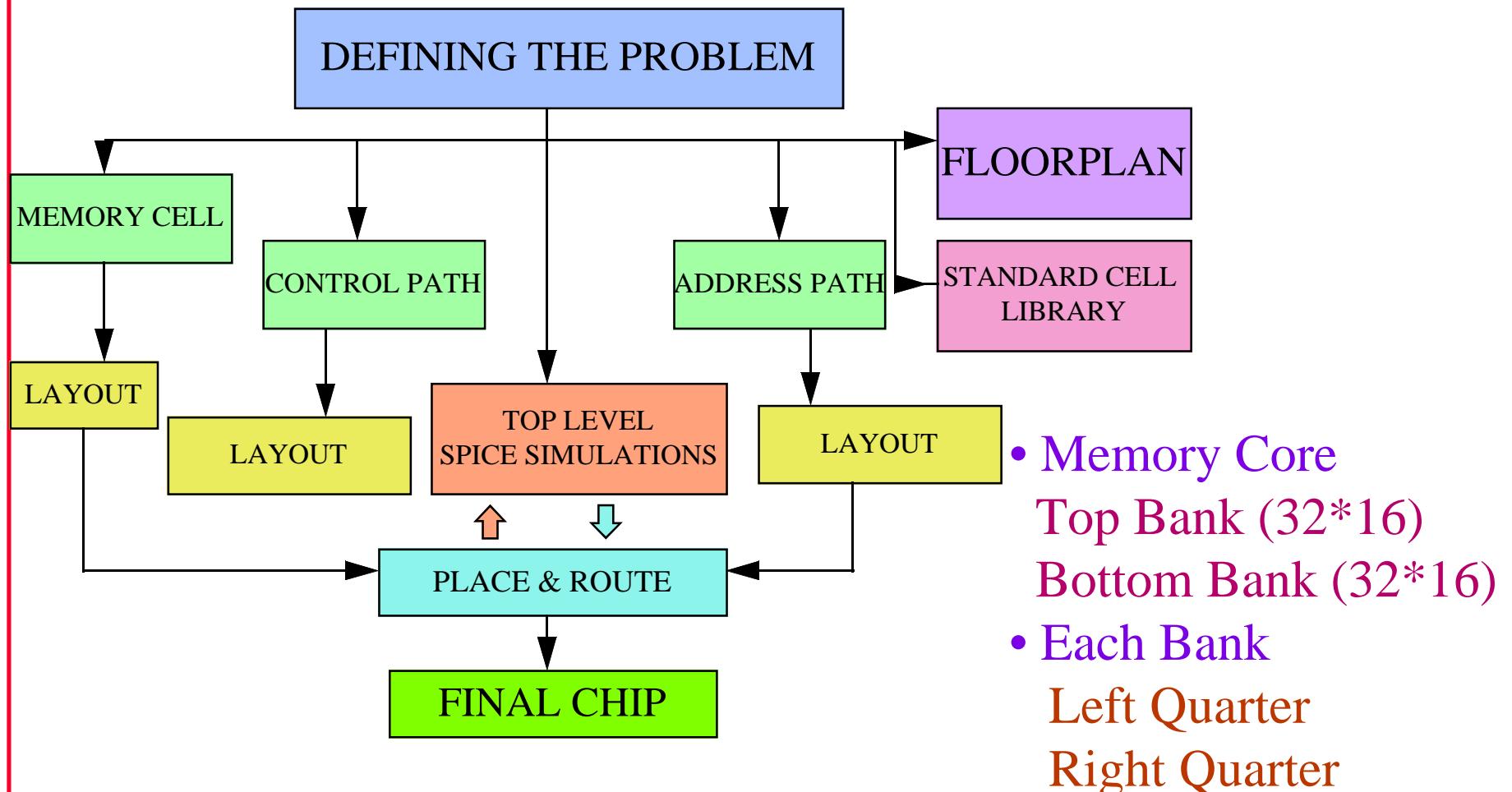


EECS 467: Introduction to VLSI Design

- Class Registration: 30
- Tools in Use: Saber, Cadence, Silvaco
- Project: Design of 64 x 16 3-T DRAM Memory
Using 0.5 mm HP MOSIS Technology
 - Design of DRAM to achieve a worst-case read access time of 20 ns, while minimizing power consumption and chip area.



EECS 467: Introduction to VLSI Design

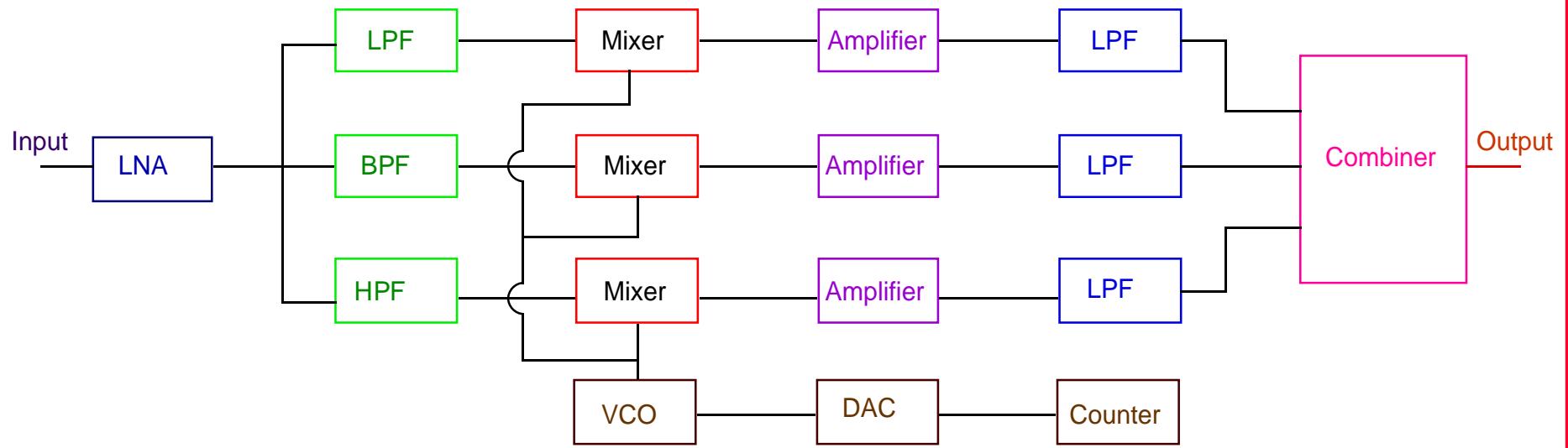




EECS 468: Analog & Mixed-Signal VLSI Design

- Class Registration: 15
- Tools in Use: Saber, MDS, Cadence
- Project: Design of On-Chip Spectrum Analyzer
 - Design of on-chip analog and mixed-signal circuitry to identify frequency components of a signal in the frequency range from 50 MHz to 150 MHz.

EECS 468: Analog & Mixed Signal VLSI Design



- 1.2 μ m HP MOSIS CMOS Technology
- Display spectral content at 1 MHz interval with resolution of 100KHz
- Spectrum is split in three bands at the input
 - less than 80 MHz (LPF)
 - 80 MHz to 120 MHz (BPF)
 - more than 120 MHz (HPF)



EECS 567: Advanced VLSI Design

- Class Registration: 16
- Tools In Use: Saber, Cadence
- Project: Design of “UIC Chip” for portable telecommunications with on-chip CPU, memory, transceiver and power management units
 - Design of on-chip mixed signal circuitry to allow monolithic implementation of analog and digital applications, along with on-chip power management and distribution



UICchip Specifications

50 MHz 8-bit RISC microprocessor with on-chip 256B memory and 400 MHz RF transceiver, and built-in power management

- 8-bit integer ALU
- 13 8-bit general purpose and dedicated registers
- 256B of on-chip program memory (SRAM)
- 28x25 bit ROM for microcode
- interrupt-driven RF I/O controller
- two-phase nonoverlapping 50 MHz clock, generated on-chip
- on-chip bandpass and lowpass filters
- frequency to voltage converter (FVC) and voltage to frequency converter (VFC) for RF signal coding and decoding
- up mixer and down mixer: direct conversion between 400 MHz and the 10 kHz – 100 kHz baseband
- RF amplifier: from 250 mV to 40 mV, at 400 MHz
- power amplifier: from 50 mV to 3.1 V, at 400 MHz
- baseband amplifier: from 20 mV to 0.55 V, at 10 kHz to 100 kHz
- 5 V and 10 V regulated power supplies, each with 5% ripple, from 5 V battery with 20% ripple
- near-zero temperature coefficient 2.5 V voltage reference